A Neural Network Based Background Calibration for Pipelined-SAR ADCs at Low Hardware Cost

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Abstract

This paper proposes a background calibration scheme for the pipelined-SAR ADC based on the neural network. Due to the nonlinear function fitting capability of the neural network, the linearity of the ADC is improved effectively. However, the hardware complexity of the neural network limits its application and promotion in ADC calibration. Hence, this paper also presents the optimization schemes, including the neuron-based sharing neural network and the partially binarized with fixed neural network, in terms of calibration architecture and algorithm. A 60 MS/s 14-bit pipelined-SAR ADC prototyped in 28-nm technology is utilized to verify the feasibility of the proposed calibration method. The measurement results show that the proposed calibration enhances the SFDR and SNDR from 68.3 dB and 44.6 dB to 95.4 dB and 65.4 dB at low frequency, and from 56.8 dB and 35.6 dB to 90.6 dB and 63.6 dB at Nyquist frequency. Meanwhile, the original calibrator and improved calibrator are synthesized in Synopsys Design Compiler to compare their hardware complexity. Compared with the unoptimized version, the optimized schemes can decrease the logic area and the network weights up to 76% and 52%, with negligible loss in calibration performance.

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Introduction: Along with the requirements for information transmission increasing, the demand for performance of the analog circuit rises rapidly. Pipelined-SAR ADC combines the advantages of pipelined ADC and SAR ADC, which gives it the advantage of high speed and high precision at the same time [1], it has many errors that need to be calibrated. The split architecture splits the normal single channel into two channels with each one just half of the original channel making its calibration diversified, simple, and efficient [2]. However, the non-ideal model of the ADC is determined by prior knowledge from the designer, the digital algorithm can only calibrate the parameters included in that model. As for the non-idealities beyond the model, the calibration is helpless.

The neural network, which has been extensively used in various fields [3] in the past decades, the digital part can be a black box with less prior knowledge of the front-end ADC. However, it suffers from considerable hardware complexity.

This paper combines the neural network and the split architecture to construct a background calibration scheme for pipelined-SAR ADC. To overcome the characteristic of high hardware complexity of the neural network, some optimizations on the calibration architecture are proposed.

Neural network based calibration: In [4], we present a machine learning based priorknowledge-free calibration scheme for pipelined-SAR ADCs with open-loop residual amplifiers. The scheme has been verified by an ADC prototype. A 14-bit 60-MSps split pipelined-SAR ADC with gain boosted dynamic amplifiers is fabricated in 28nm CMOS to validate the scheme. The measurement results show the ADC achieves an SFDR of 93.7 dB and an ENOB of 10.7b, consuming 2.79 mW.

Fig. 1 presents the calibration architecture based on the neural network. A normal pipelined-SAR ADC is split into two theoretically identical channels, ADCA and ADCB. Taking channel A as an example. The corrected ADC output O_A is obtained by adding two different parts. The first is the ideal-weight combiner output, namely the sum of each comparison result multiplied by its corresponding weight. Generally, it is the exact ADC output. The second is the output of the neural network O_A^2. The difference between channels ΔA is employed to train the neural network, and the average of O_A and O_B is used as the calibrated output.

Fig. 2 shows the structure of the neural network in Fig. 1 which is called the full-precision neural network (FPNN). Channel A is used as a demonstration. The two-layer network consists of input and output layers. Neurons have activation function which rectified linear unit (ReLU) is usually used due to its low hardware complexity. D_n and $N_i$represent n-th digital input and i-th neuron. $W_{i,n}^1$ represents the n-th weight of i-th neuron in the input layer and W_i^2 represents the weight of i-th neuron in the output layer. The input of neural network is binary digital code output generated by all comparators in ADCs.

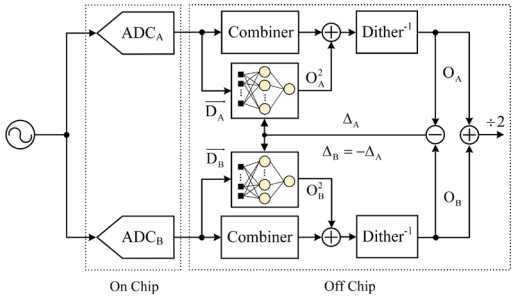

Fig. 1 *The proposed calibration architecture (modified from [4]).*

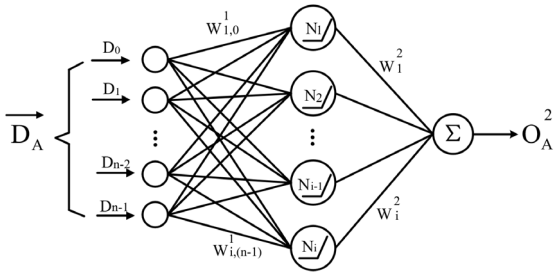

Fig. 2 *The structure of full-precision neural network.*

Even though neural-network-based ADC calibration works well in performance improvement, it suffers from considerable hardware complexity. Aiming to promote the application of this method, the next section will focus on the optimization schemes for the calibrator.

The hardware optimization: The goal of this section is to simplify the hardware of the calibrator with little loss of calibration performance. In the calibration system of Fig. 2, the neurons and weight directly affect the capacity of the memory, and the multiplier in the output layer affects the area and power consumption. In addition, both fully parallel and fully serial architectures have certain drawbacks. Based on the idea above, several methods for optimizing hardware. As a result, the optimized schemes greatly simplify the hardware.

Due to the similarity between two channels, they can share a portion of neural network weights to further optimize hardware resources. Fig. 3(a) demonstrates a neuron-based sharing neural network (NSNN) sharing mechanism where neurons in green and their weights are shared, while those in black are owned by channel independently. $Wd_{n,m}^1$ represents the i-th weight of m-th independent neuron and $Ws_{n,k}^1$ represents the i-th weight of k-th shared neuron in the input layer. Wd_m^2 represents the weight of m-th independent neuron and Wd_k^2 represents the weight of k-th shared neuron in the output layer. The sum of m and k is the total number of neurons i. Sharing rate is defined as the ratio of shared neurons to total neurons. It is appropriate to choose a sharing rate of 25% through simulation.

As mentioned, multipliers in the output layer account for the majority of area and power consumption. To reduce power consumption and the area of the multiplier, the partially binarized with fixed neural network (PBFNN) structure is proposed in Fig. 3(b). In that figure, W_n is the binarization of output layer weight. The operation, binarize, is to constrain the weights to 0 and 1, and fix, which means that the output layer no longer performs backpropagation. Therefore, multipliers can be replaced by data selectors in green. It is a mathematical abstraction of the data selectors, which is characterized by (1) Where Y_j represents the input of i-th neurons. The reduction in quantization bits of output layer weight may cause a decrease in calibration performance. But through simulation, the impact can be ignored due to the reduction in area and power consumption. Therefore, Both memory and logic benefit from the PBFNN.

$$\text{sel}(Y,W) = \begin{cases} Y_j, W_i^2 = 1 \\ -Y_j, W_i^2 = 0 \end{cases} \quad (1)$$

In addition, an appropriate reduction in the number of neurons and. local Parallel Implementation can achieve a trade-off between calibration performance and power. Therefore, NSNN and FBFNN structure will be implemented using 16 neurons and a local parallel architecture.

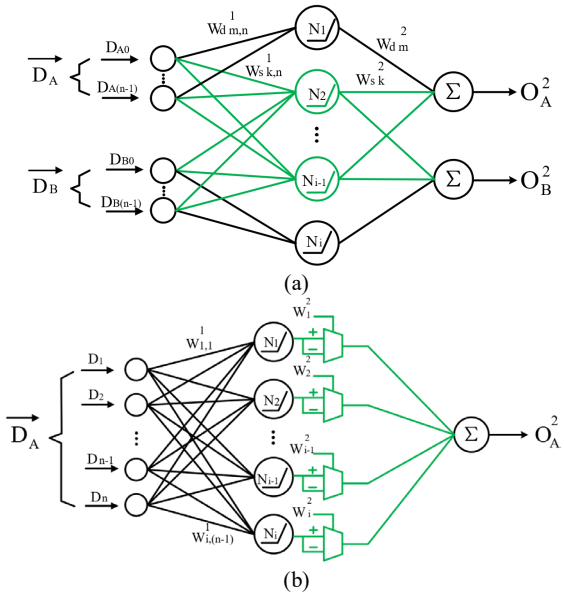

Fig. 3 *(a) The structure of Neuron-based Sharing Neuron Network (b) The structure of partially binarized with fixed neural network.*

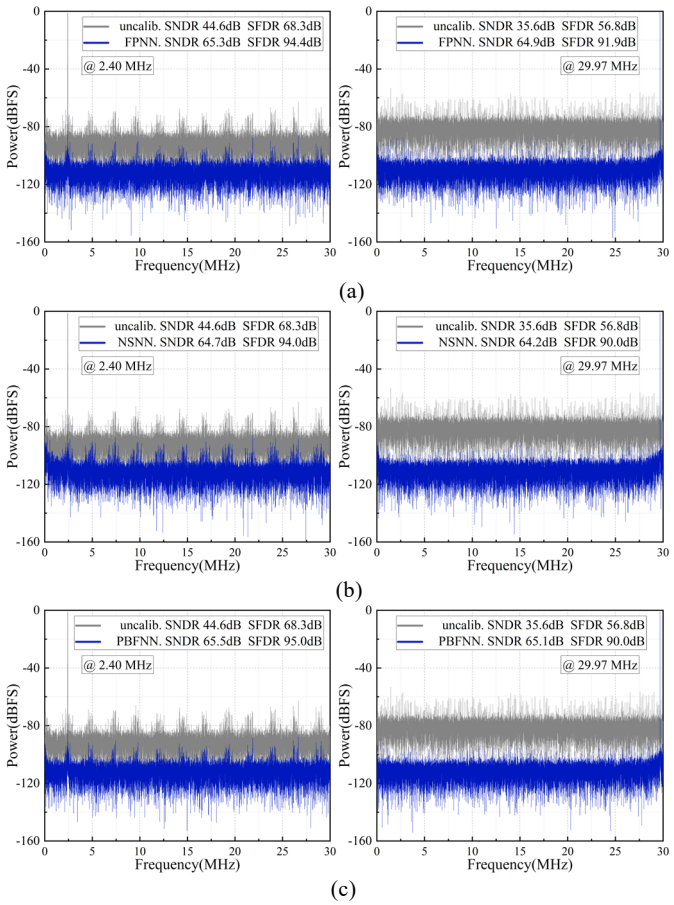

Fig. 4 *The measured FFT spectrums before and after calibration with the FPNN (a), the NSNN (b), the PBFNN (c) at low frequency and Nyquist frequency.*

Measurement results: This section intends to verify whether the improved versions can optimize the hardware with an acceptable performance penalty. A 14-bit pipelined-SAR ADC prototyped with a sampling rate of 60 MS/s is employed [4]. The Synopsys Design Compiler is utilized to compare the hardware complexity before and after optimization. 16 neurons and a 25% sharing rate are designed in this experiment.

Fig. 4 shows the FFT spectrums at low frequency (2.40 MHz) and Nyquist frequency (29.97 MHz) before and after calibration using three proposed schemes including the FPNN, the NSNN, and the PBFNN. The SFDR and SNDR of the uncalibrated ADC at low frequency are 44.6 dB and 68.3 dB, and those at Nyquist frequency are 35.6 dB and 56.8 dB. After calibration, the SFDR and SNDR are optimized up to approximately 95 dB and 65 dB at low frequency, and 90 dB and 65 dB at Nyquist frequency. It proves that the optimized calibration versions also perform well in the refinement of the ADC performance.

TABLE 1: Comparison with other ADCs

	[5]	[1]	[2]	This work
ADC architecture	SAR	PPL-SAR	PPL-SAR	PPL-SAR
frequency (MS/s)	160	500	60	60
resolution (bit)	12	11.5	14	14
method	PRBS	Aux.	Split	Split
algorithm	LMS	LMS	LMS	NN
SFDR@low(dB)	86.9	N.A.	91.0	95.4
SNDR@low(dB)	N.A.	N.A.	66.9	65.4
SFDR@nyq.(dB)	84.9	75.5	84.1	90.6
SNDR@nyq.(dB)	65.3	62.3	64.1	63.6

TABLE 2: Comparison between calibration schemes

	FPNN	PBFNN	NSNN
SFDR(dB)	94.4	95.0	93.4
SNDR(dB)	65.3	65.0	65.2
Weight number	430	396	204
logic area(um^2)	36161	10143	8413

Table 1 summarizes this work and compares it with other state-of-art ADCs. As with other advanced techniques, the improvement in linearity at both low frequency and Nyquist frequency. Furthermore, the linearity at Nyquist frequency is close to that at low frequency in this work.

Table 2 compares the calibration performance and hardware complexity. The FPNN consumes a huge logic area due to the employment of the multipliers, and it is optimized by about 72% by the multiplier-free PBFNN. The NSNN shares the neuron weight, hence optimizing the weights and logic by approximately 52% and 76% compared to the FPNN. Moreover, in these improved schemes, the performance of the calibrated ADC is nearly lossless.

Conclusion: In this paper, the calibration method for the pipelined-SAR ADC based on the neural network is introduced. Meanwhile, optimization schemes are proposed to simplify the hardware complexity. A 60 MS/s 14-bit pipelined-SAR ADC is used to verify the effectiveness of the calibrations before and after improvements, and the Synopsys Design Compiler is exploited to obtain their logic areas. The measurement results show that the proposed calibration schemes can efficiently refine the ADC performance, especially the linearity. Moreover, the optimized schemes greatly simplify the hardware with negligible loss in calibration performance.

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