Analysis of Etched drain based Cyl GAA TFET based SRAM cell Design

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Abstract

This paper aims to propose a novel method for designing an SRAM cell using an Etched Drain based Cyl. GAA TFET with a hetero-substrate material and an elevated density strip. The aim is to reduce power dissipation and improve stability, as demonstrated through analysis utilizing SNM as well as N-Curve methods. With respect to the 16nm MOSFET based SRAM cell, the proposed device-based SRAM cell shows significant improvements with a 68.305% reduction in leakage power, a 15.58% increase in SVNM, an 8.623% increase in SINM, an 8.152% increase in WTV, a 12.86% increase in WTI, a 27.62% increase in SPNM, and a 19.95% increase in WTP. The design is implemented and analyzed using Cadence Virtuoso software, and a novel approach of look up tables and Verilog A is utilized for the device to circuit application. These results indicate promising advancements in the design of SRAM cells, which could have significant implications for the development of advanced computer systems.

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Abstract — This paper aims to propose a novel method for designing an SRAM cell using an Etched Drain based Cyl. GAA TFET with a hetero-substrate material and an elevated density strip. The aim is to reduce power dissipation and improve stability, as demonstrated through analysis utilizing SNM as well as N-Curve methods. With respect to the 16nm MOSFET based SRAM cell, the proposed device-based SRAM cell shows significant improvements with a 68.305% reduction in leakage power, a 15.58% increase in SVNM, an 8.623% increase in SINM, an 8.152% increase in WTV, a 12.86% increase in WTI, a 27.62% increase in SPNM, and a 19.95% increase in WTP. The design is implemented and analyzed using Cadence Virtuoso software, and a novel approach of look up tables and Verilog A is utilized for the device to circuit application. These results indicate promising advancements in the design of SRAM cells, which could have significant implications for the development of advanced computer systems.

Keywords— Tunnel Field Effect Transistor (TFET), Static Random Access Memory (SRAM), Static Noise Margin (SNM), Static Voltage Noise Margin(SVNM), Static Current Voltage Margin(SIVM), Write Trip Voltage(WTV), Wire Trip Current(WTI)

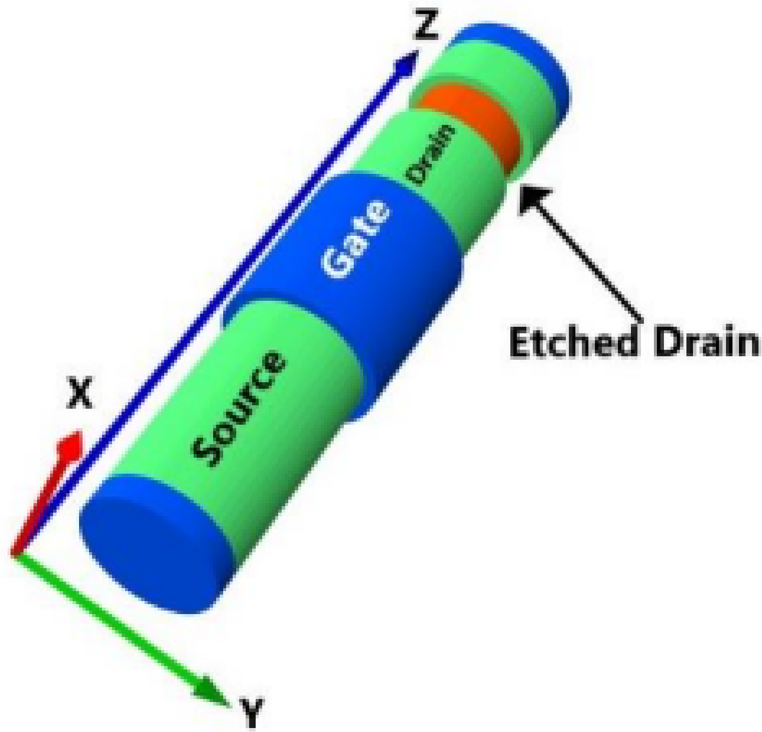
Introduction

The packing density of the integrated circuits has increased due to the growth witnessed by the semiconductor industry, resulting in smaller components and transistors. One of the crucial components in modern day electronics is the Static Random-Access Memory cell, but the higher integration density required for compact memory cell design comes at a cost of increased leakage current. Standby leakage is a major contributor to total leakage in low-tech systems, and it significantly impacts battery life in portable devices. To reduce leakage, the circuit operates at a lower supply voltage, However, this impedes the circuit's speed. Lowering the threshold voltage of transistors reduces delay but increases leakage, particularly sub-threshold leakage. Design improvement is important to achieve a memory cell with reduced standby leakage and improved stability in the face of smaller size and lower voltages.

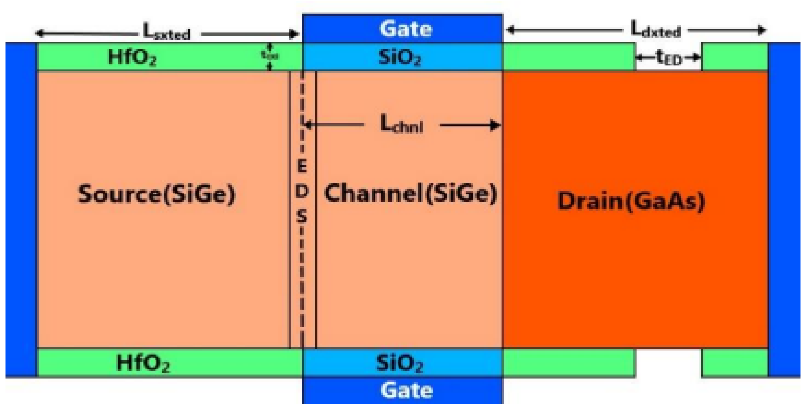
To address this constraint, SRAM cell design has been implemented using Etched Drain based GAA TFET technology, resulting in low power dissipation and better stability. This design detects Ioff of 1.51 x 10^{-19} A/um at $V_{GS} = 1.5$V, Subthreshold Swing (SS) of 35mV/decade, and I_{on}/I_{off}greater than 10^{14} for a threshold voltage of 0.5V. Stability analysis is conducted using the N-curve method in the Cadence Virtuoso Environment, using a Verilog A models rooted upon utilization of lookup tables. In summary, the semiconductor industry's growth has resulted in smaller components and transistors, requiring a more compact memory cell design. However, this comes at a cost of increased leakage current. The new SRAM cell design using Etched Drain Based GAA TFET technology aims to address this constraint by reducing power dissipation and improving stability, making it a promising solution for the next generation of electronic devices. The focus of this paper is that we are using a novel approach of implementing SRAM cell using Etched Drain based Cyl. GAA TFET. The device to circuit application is based on look up tables and Verilog A approach.

Tcad Device Modelling

In order to model the device accurately using TCAD Synopsys, we utilized the following parameters: an Etched Drain Thickness (t_{ed}) of 5nm, an Oxide thickness (t_{oxi}) of 2nm, a channel length (L_{chnl}) of 30nm, radii (R) of 7nm, and a gate work function of 4.8 eV (Tungsten diSilicide). The P^{++} doped (elevated doped) ESD was set to a concentration of $10^{20}/cm^3$, while the P^+ channel was doped at a concentration of $10^{15}/cm^3$, and the P^+ source at a concentration of $10^{18}/cm^3$. The N^+drain was doped at a concentration of $5x10^{17}/cm^3$ [1]. The extended length for the source (L_{sxted}) and drain (L_{dxted}) was set to 40nm. To measure the effect of I_{OFF}, we employed a non-local BTBT model and a trap assisted tunneling model, while the Shockley Read Hall (SRH) model was employed to estimate fixed minority carrier's lifetime.



(a)



(b)

Fig. 1. a) 3D representation, and (b) 2D Cutline representation of Cyl. GAA etched drain based TFET [1]

Device to circuit application

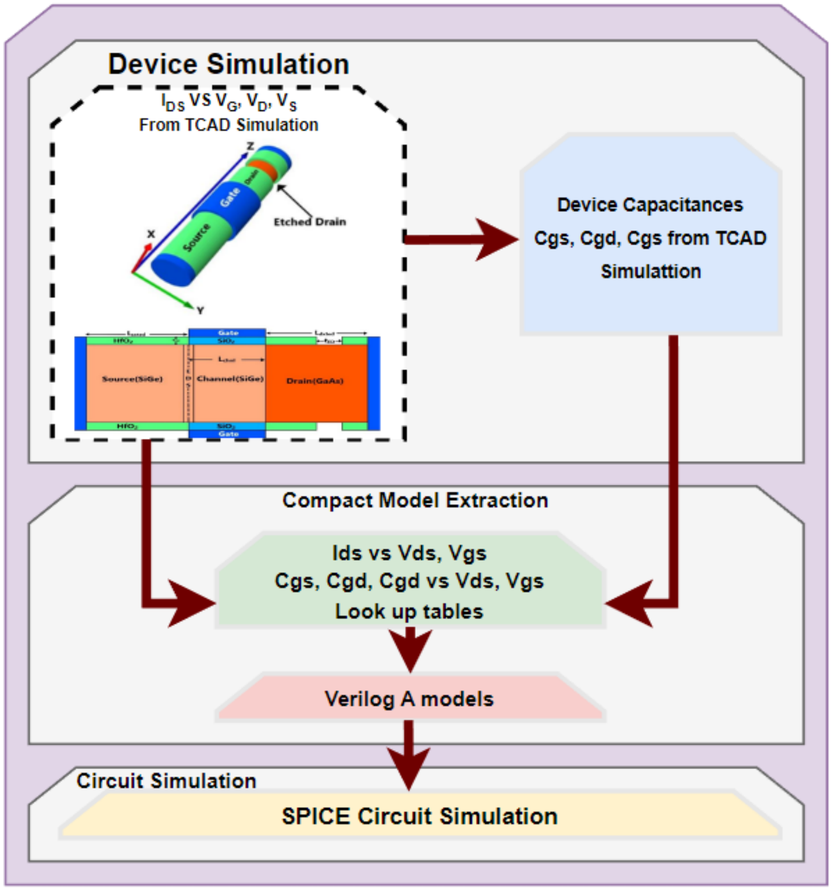


Fig. 2. Device to circuit application algorithm

To address the lack of accurate analytical models for Etched Drain based GAA TFET, utilizing a Verilog-A device model designed utilizing lookup table, we were able to achieve both precision and efficiency in compact modeling for emerging devices. Verification against conventional BSIM modeling confirms the validity of this approach and is shown in the figure above, which outlines the simulation methodology used in this study. To implement this model, we first optimized various parameters through device simulation. We then generated lookup tables for I_{ds}, C_{gs}, and C_{gd} in terms of V_{gs} and V_{ds} using the obtained I–V and C–V graphs. By integrating these lookup tables into Verilog-A-based models, they can be employed in conjunction with SPICE simulation. Lastly, the Cadence Virtuoso tool was utilized to conduct simulations and measurements of diverse performance metrics for the SRAM circuit.

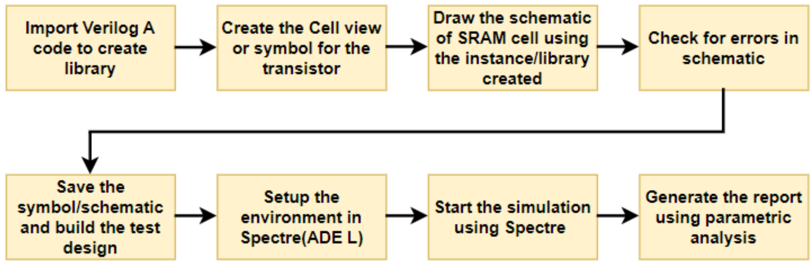


Fig. 3. Cadence Virtuoso Design Flow

Our primary goal is to import the Verilog A code and utilize it to create a transistor cell view and a library. Subsequently, we will employ this cell view to develop the SRAM cell. We will meticulously scrutinize the schematic for any discrepancies. Afterward, we will proceed to create the test design and configure the environment in Spectre ADE L. Once we have set up the environment, we will execute the simulation using Spectre and obtain the necessary results or report.

6T SRAM Cell

SRAM (Static Random-Access Memory) is a type of computer memory that stores data using flip-flop circuits, providing fast access speeds and retaining data as long as power is supplied.

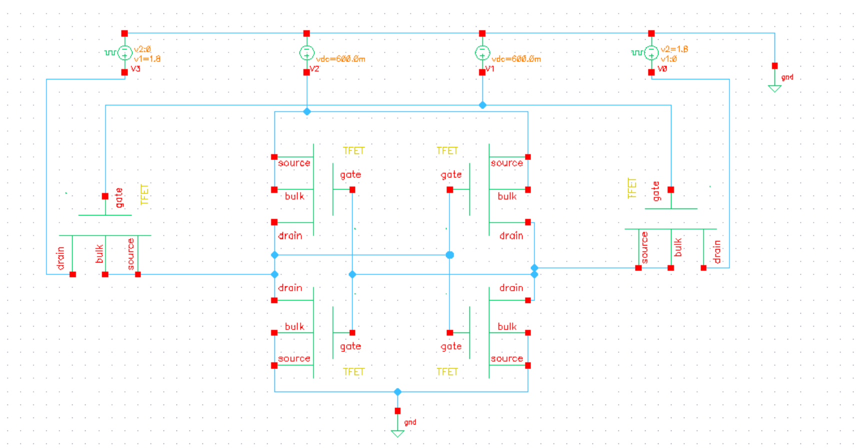


Fig. 4. 6T SRAM cell

Stability Metrics

The objective pertaining to this paper implies to explore the suitability of two methods, namely the SNM metric and N curve method, for evaluating the reliability concerning an Static Random Access Memory cell. Emphasis is placed on the N curve method due to the drawbacks associated with using the SNM metric butterfly curves approach, a restrictive factor constitutes incapability with the intention of automatically measuring the SNM using inline testers, time-consuming mathematical calculations, and imprecise results due to the need to fit squares in each lobe to determine the SNM. Therefore, the N curve method is considered more appropriate as it offers higher accuracy and does not require complex mathematical calculations.

Results

Static Noise Margin

The primary determinant of an SRAM cell's stability is its capacity to withstand and maintain reliable operation when subjected to high levels of DC noise voltage, which is commonly referred to as the SNM (Static Noise Margin).

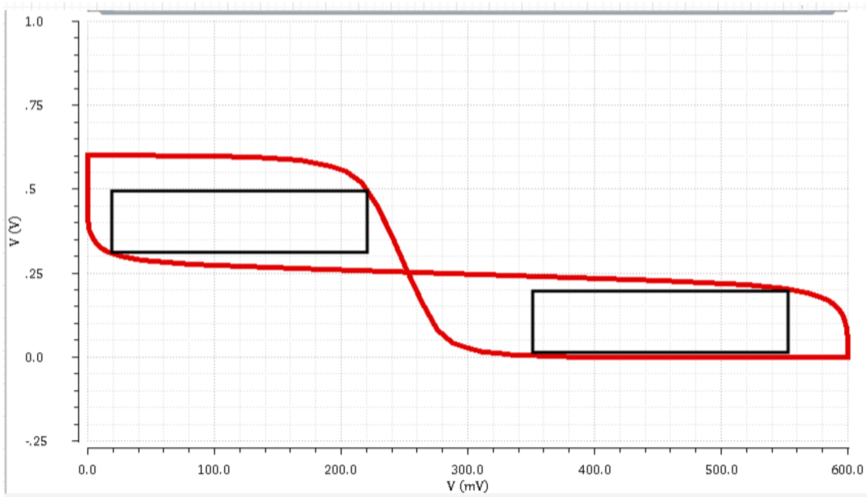


Fig. 5. Hold Static Noise Margin

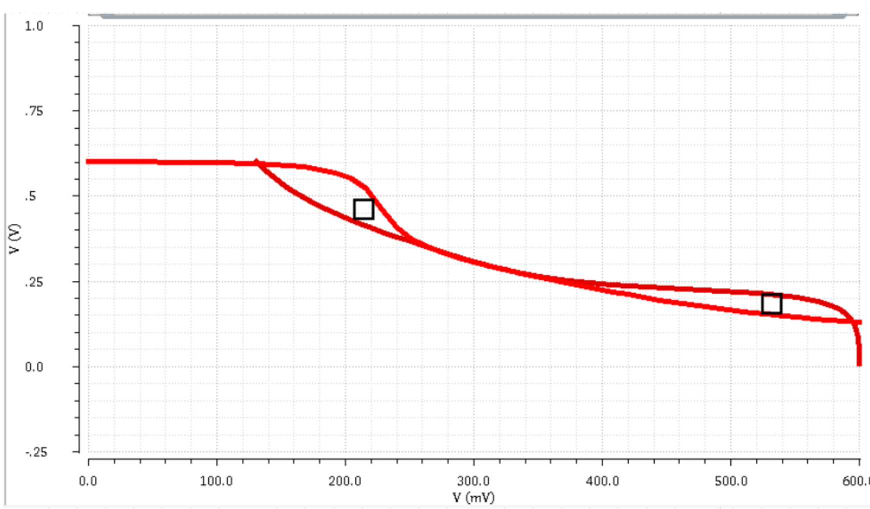


Fig. 6. Read Static Noise Margin

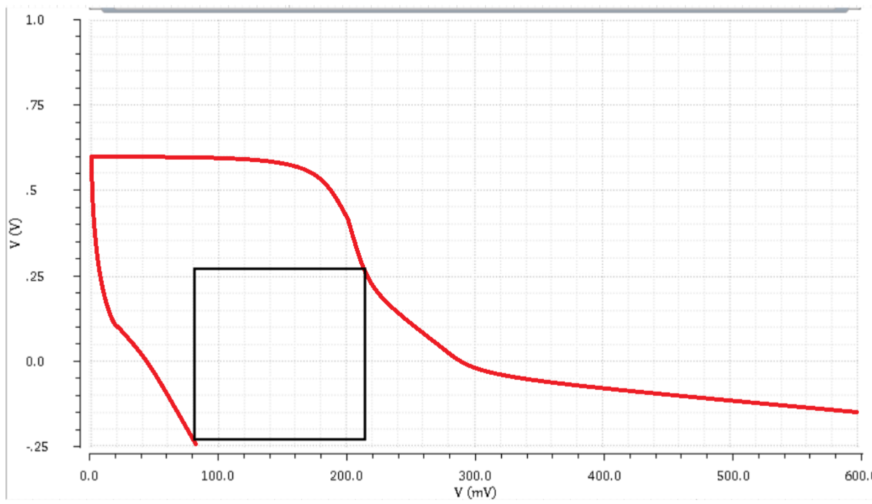


Fig. 7. Write Static Noise Margin

N-Curve Metric

The N curve metric is utilized by inline testers to gather information for both current and voltage. Unlike the VTC approach, this metric does not have a voltage scaling delimiter and encapsulates all stability information within a single plot.

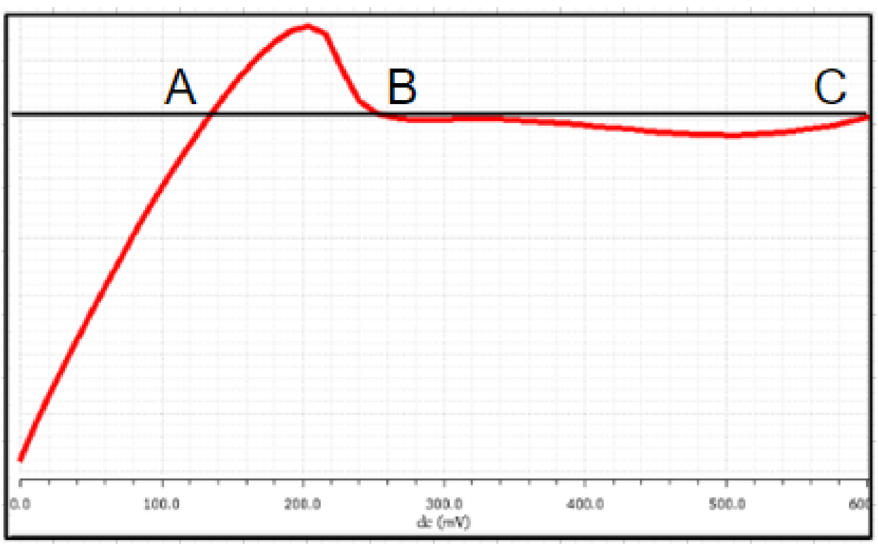


Fig. 8. N-Curve for stability analysis

Static Voltage Noise Margin (SVNM)

The SVNM refers to the maximum threshold of DC noise voltage that an SRAM cell's inverter input can endure without inducing any alteration in its stored data. The simulation plot presented in Figure IV(e), the voltage disparity between points A and B is depicted, showcasing the maximum permissible DC noise voltage that the SRAM cell can endure while preserving the integrity of its stored data. In simpler terms, SVNM serves as a measure of the SRAM cell's stability against external noise disturbances.

SVNM = V_B - V_A

Static Current Noise Margin (SINM)

The SINM is an essential parameter that evaluates the stability of the SRAM cell under the influence of external current disturbances. It represents the maximum allowable DC current that can be injected into the cell without causing any modification to its stored data. The accompanying plot depicts the peak current positioned between points A and B, providing insight into the SRAM cell's ability to withstand current interference while preserving data integrity. By measuring SINM, we can ensure that the SRAM cell can withstand external current noise and maintain its stored data, thus evaluating its stability.

Write Trip Voltage (WTV)

The WTV denotes the minimum voltage reduction required to switch the internal node "1" of the SRAM cell from one state to another, while both bit lines are held at the Vdd voltage level. This value can be determined by measuring the voltage discrepancy between points C and B in the corresponding plot, as depicted in Figure IV(e). Through the measurement of the WTV, we can evaluate the essential voltage required for writing data into the SRAM cell. This information is crucial for assessing the functionality and performance of the cell. The WTV serves as a critical parameter in assessing the SRAM cell's write ability, ensuring accurate and reliable data storage operations. In other words, WTV indicates the voltage threshold at which the SRAM cell can be successfully programmed with a new data bit.

SVNM = $V_B - V_C$

Write Trip Current (WTI)

WTI refers to the minimum current level necessary to write data into the SRAM cell without causing any undesired disruptions. It can be determined by identifying the negative peak current between points C and B in the N-curve illustrated in Figure IV(e). The overlapping of points A and B, or B and C, can compromise the stability of the SRAM cell. Hence, WTI serves as a crucial metric for evaluating the write capability of the SRAM cell, ensuring accurate and reliable data writing while preserving its stability. In essence, WTI specifies the minimum current required to change the state of the SRAM cell without any unwanted disturbances.

Power Dissipation for various Technologies

Technology (nm)	45	32	22	16	30 (TFET)
Static Power Dissipation (pW)	12.991	15.773	23.782	46.348	0.0262
Dynamic Power Dissipation (nW)	4.720	2.103	0.910	0.36	0.1047
Total Power Dissipation (nW)	4.733	2.119	0.934	0.413	0.1309

The reference values presented in the table for the MOSFET based SRAM power dissipation has been referred from [8]. With reference to these values, Etched drain-based GAA TFET based SRAM power dissipation has been compared.

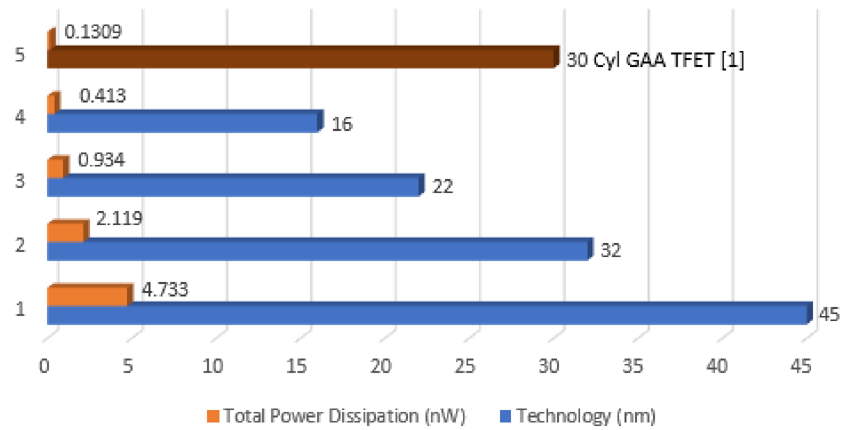


Fig. 9. Total Power Dissipation for MOSFET vs TFET

Stability Metrics for MOSFET based SRAM vs TFET based SRAM

Parameters	Typical 6T SRAM	TFET based SRAM	Growth
Process	45nm/1V, 27	30nm/1V, 27	-
Stability Metric	N-Curve	N-Curve	-
SVNM	320.9mV	405.16mV	15.58%
SINM	181.2µA	198.3µA	8.623%
WTV	547.5mV	596.1mV	8.152%
WTI	-78.96µA	-90.62µA	12.86%
SPNM	58.147µW	80.343µW	27.62%
WTP	-43.23µW	-54.01µW	19.95%

The reference values presented in the table for the MOSFET based SRAM power Stability Metrics has been referred from [9]. With reference to these values, Etched drain-based GAA TFET based SRAM Stability Metrics has been compared.

Conclusion

Our study involves the implementation of 6T SRAM using Etched drain based Cylindrical GAA TFET and its analysis. The stability of the SRAM cell was assessed through the utilization of the N-Curve Method, allowing for a comparison of its leakage power with MOSFETs employing different technological variations. Our results indicate that our system has a 68.3% reduction in leakage power dissipation compared to a 16nm MOSFET. Moreover, we achieved improvements in several key parameters such as a 15.58% increase in SVNM, 8.623% increase in SINM, 8.152% increase in WTV, 12.86% increase in WTI, 27.62% increase in SPNM and 19.95% increase in WTP. Overall, our Etched Drain based Cyl. GAA TFET based SRAM cell exhibits superior stability and lower leakage power dissipation.

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