Low frequency operation and micro-controller implementation for multilevel quasi Z source inverter in photovoltaic application

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Abstract: - A microcontroller based pulse width modulation implementation for multilevel quasi Z source inverter is proposed in this paper. The component design of quasi z source inverter (qZSI) is first considered with continuous and discontinuous mode of operations. The low switching frequency operation of multilevel quasi Z source inverter is proposed in this paper. The detailed modelling for qZSI is then established for effective implementation of PIC microcontroller (PIC 16F877A) for generating the switching signals. A prototype of five level quasi z-source inverter have been developed and the control signal to the gate drivers have been applied by properly adjusting the shoot through and non shoot through switching states. The hardware result shows the effective implementation of the proposed scheme.

Key-Words: - Quasi-z source inverter, Pulse width modulation, PIC microcontroller, multi level inverter, solar photovoltaic, shoot through state

1 Introduction

With the increasing dependence on photovoltaic (PV) system in grid connection mode, there is a sharp rise in the advancement of multilevel inverter applications. Among the various multilevel inverter topologies, the cascaded H-bridge multi level inverter (CHB) and diode clamped multilevel inverter (DCMI) are the most common configurations which have been area of active research. As compared with the conventional two level inverter topologies, the output voltage waveform in multilevel inverter have several voltage levels with small voltage steps generated from small rating semiconductor switches and thus leading to lower THD and less $\frac{dV}{dt}$ stress. For high voltage output, the CHB and DCMI requires large number of modules, more switches and more number of gate drivers and thus leading to increased cost and complexity [1-2]. To overcome this limitation, the high gain Z-source inverter and quasi Z-source (QZS) inverter have gained importance in the multilevel inverter configuration, where dc link voltages have been boosted with the help of an LC based network. The DC link of conventional VSI is replaced by Z source impedance network in Z-source inverter & Quasi Z-source inverter which not only provide an additional stage of DC-DC boost to output voltage but also creates new switching state i.e. shoot through states [3-4]. These inverters also provide protective enhancement of the switches without affecting the overall cost and efficiency. Areas such as solar photovoltaic, fuel cell stack and batteries which require high voltage gain, extract the advantage of ZSI/QZSI. Multilevel ZSI/QZSI are best suited for high voltage & high power demand as the number of inverter voltage increases, output ac waveform have low distortion with reduced blocking voltage across each switch. New PWM techniques based on phase disposition (PD) have been developed for multilevel configurations of ZSI/QZSI in order to have the gain through shoot through. In [3-4], the PD scheme for three levels NPC- ZSI which infers the boosted output voltage with less number commuted switch count have been discussed. Similarly [5]-[6] analyse three level NPC- QZSI which provide continuous dc source current along with good boost factor.

A 9-level inverter design combining hybrid three-level modified-QZSI with a single-phase modified-QZSI has been investigated in [7]. A significant boost of almost three times of dc link voltage of each cell and

THD level of approximately 3% have been reported from the simulation & experimental results. A new five level QZS -NPC inverter is proposed in [8] having a level shifted carrier wave. The simulated results infer high

Table: I Comparison of number of components

Components	DC/DC Converter	Z-source	Quasi Z-source
Switches	$\frac{3m+5}{2}$	$m+3$	$m+3$
Capacitors and inductors	$m-1$	$2(m-1)$	$2(m-1)$
Diodes	$\frac{m-1}{2}$	$\frac{m-1}{2}$	$\frac{m-1}{2}$

boosted output voltage and good reactive power capability but it's not validated experimentally. Table I summarizes the required number of switches, total number of capacitors and inductors, and total number of diodes for the three introduced multilevel inverters at a specific number of output voltage levels (m). A two stage control method is proposed in [9] for QZSI to control the output voltage & current. It also concludes that capacitor voltage controller for ZSI/QZSI is preferred above dc link controller for conventional VSI to boost output voltage. An inverted phase shifted PWM scheme is employed for a five-level grid connected QZSI injecting power into the PV- grid at reduced THD level is worked in [10]. The power is controlled using dc link controller & independent MPPT control. The low switching frequency reduces the switching losses considerably and thus very much suitable for medium voltage high power applications [11-12]. The application of qZSI have been worked out in various literature considering the improvements in various parameters in [13-19]

In this paper the low switching frequency operation of quasi Z source based multilevel inverter configuration for solar photovoltaic operation is proposed. The proposed model have been implemented using the dspic based microcontroller (PIC 16F877A). The paper is arranged as follows: section 2 discusses the fundamentals of matrix converter. In section 3 the harmonics minimization equations are formed by using Fourier series analysis. Section 4 describes the differential evolution optimization technique for obtaining the switching instants of the objective function derived in section 3. Analytical and computational results are presented in section 5. Experimental results from a prototype to validate the analytical and computational results are given in section 6. Finally conclusion of the work is presented in section 7.

2 Mathematical modelling

Solar Cell:

Solar panels are constructed with solar cells as basic component. Several solar cells are connected in series and parallel in order to achieve desired voltage and currents at the output. The single diode model of a single solar cell is the combination of a diode, two resistors and a current source. To obtain the I-V, characteristics, the required expression can be derived and can be expressed by (1). From the expression, it is clear that the photo current depends on the solar irradiance and cell temperature and therefore, it can be represented by (2).

$$I_{ph}=\left[I_{sc}+k_i\cdot(T-298)\right]\cdot\frac{G}{1000} \tag{1}$$

$$I_O=I_{rs}\cdot\left(\frac{T}{T_n}\right)^3\cdot\exp\left[\frac{q\cdot E_{go}\cdot\left(1/T_n-1/T\right)}{n\cdot K}\right] \tag{2}$$

Here I_{SC} is at 25˚C short circuit current, T is the cell's temperature and k_i is the short circuit current temperature coefficient. Since diode current or the cell saturation current varies with the cell temperature and is given by (3), I_{rs} is the cell's reverse saturation current at reference temperature and solar radiation and E_{go} represents the semiconductor's band gap energy utilized for manufacturing the cell. Also, the reverse saturation current is the current through the shunt resistor. The expression for the shunt current and the load current can be given by (4)-(5).

$$I_{rs} = \frac{I_{sc}}{-1 + e^{\left(\frac{q \cdot V_{oc}}{n \cdot N_S \cdot K \cdot T}\right)}} \tag{3}$$

$$I_{sh} = \left(\frac{V + I \cdot R_s}{R_{sh}}\right) \tag{4}$$

$$I = I_{ph} - I_O \cdot \left[\exp\left(\frac{q \cdot (V + I \cdot R_s)}{n \cdot K \cdot N_s \cdot T}\right) - 1\right] - I_{sh} \tag{5}$$

Where I_{ph} is the photo current or generated current, I_O is the saturation current and R_S is the series resistance. Based on the mathematical modelling of single diode photovoltaic cell, the simulation model of PV cell is developed and the I-V, PV characteristics have been shown in Fig. 1 for various values of Irradiance and temperatures.

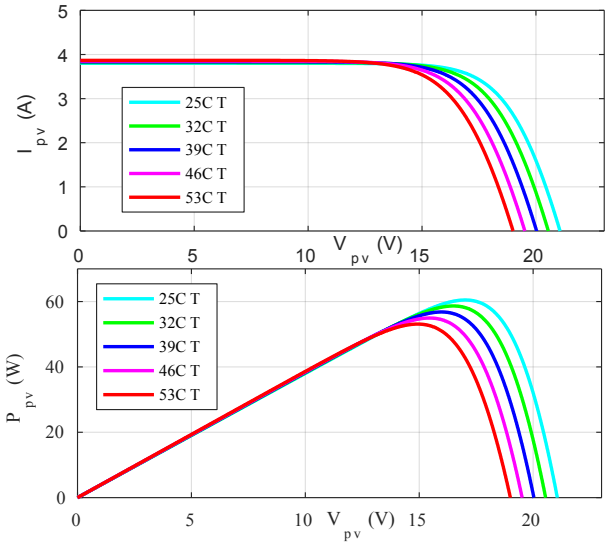


Fig. 1. *TRINA Solar TSM-250PA05.08 Characteristics*

Quasi Z source Inverter

A single stage control of buck or boost operation of voltage is achieved in quasi Z-source inverter. In qZSI topology the controlled semiconductor switches can be simultaneously turned ON in the same leg and thus provides the gain in the output voltage. Also, it will remove the requirement of the dead time in practical implementation of the converter and therefore offers simplifications in control design. The single cell of the quasi Z source inverter topology is shown in Fig.2 (a). For the construction of quasi network, two inductors and two capacitors are required. The shoot through (same switches in the leg are turned on), null state and non shoot through states or active states will charge or discharge these components based on the gain required in the output voltage. Since, in the null state, all the switches are turned off simultaneously, no power transfer from the input side to the outside takes place. The equivalent circuit [20], of the qZSI in the non-shoot-through state and the equivalent circuit of the qZSI in the shoot-through state are shown in Fig 2(b) and Fig 2(c) respectively. All the voltages as well as the currents are defined in these figures and the polarities are shown with arrows.

Assuming that during one switching cycle, T, the interval of the shoot-through state = T_0, the interval of non-shoot-through state = T_1, thus one has T =T_0+T_1, and the shoot-through duty ratio is, $D=\frac{T_0}{T}$

Thus during the interval of the non-shoot-through state,T_1, one can get as in (6) and (7).

$$V_{L1}=V_{in}-V_{C1} \quad ; \quad V_{L2}=-V_{C2} \tag{6}$$

$$V_{PN}=V_{C1}-V_{L2}=V_{C1}+V_{C2} \; ; V_{diode}=0 \tag{7}$$

During the interval of the shoot-through states, T_O, one can get (8)

$$\begin{aligned} V_{L1}&=V_{C2}+V_{in} \quad ; \quad V_{L2}=V_{C1} \\ V_{PN}&=0 \quad ; \quad V_{diode}=V_{C1}+V_{C2} \end{aligned} \tag{8}$$

At steady state, the average voltage of the inductors over one switching cycle is zero. Therefore, we get (9) and on solving we can have (10).

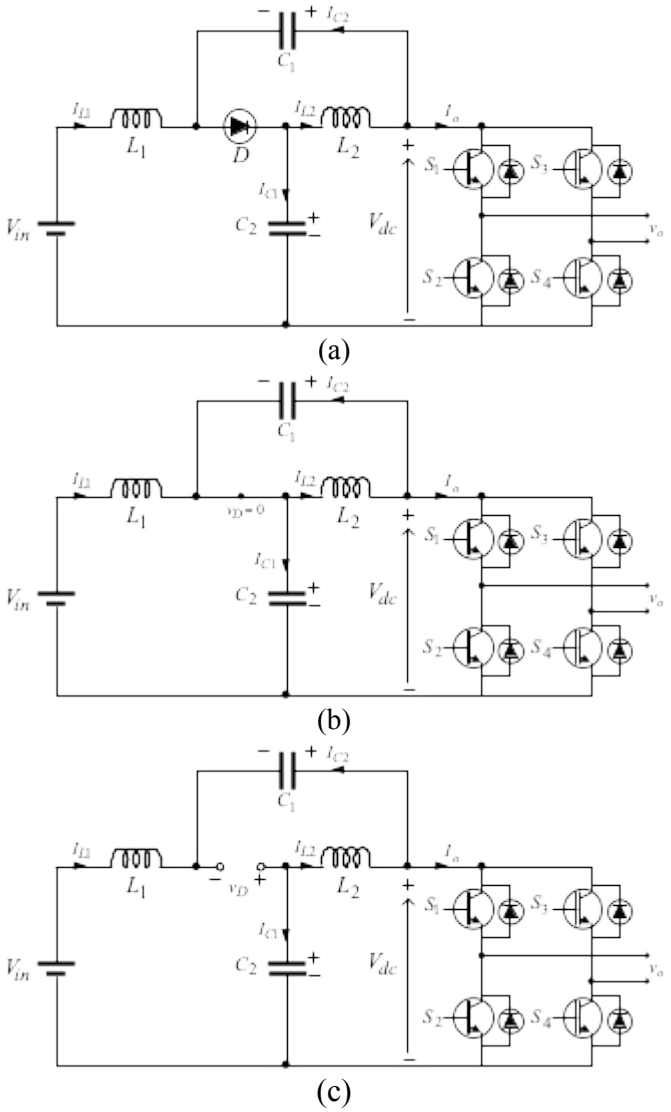


Fig2: qZSI (a) Topology (b) Non-shoot through state (c) shoot through state

(9)

$$V_{L1}=\overline{v_{L1}}=\frac{T_O\left(V_{C2}+V_{i}\right)+T_1\left(V_{i}-V_{C1}\right)}{T}=0$$
$$V_{L2}=\overline{v_{L2}}=\frac{T_O\left(V_{C1}\right)+T_1\left(-V_{C2}\right)}{T}=0$$

Thus, $$V_{C1}=\frac{T_1}{T_1-T_O}V_{i}, V_{C2}=\frac{T_O}{T_1-T_O}V_{i} \quad (10)$$

The peak dc-link voltage across the inverter bridge is,

$$V_{PNpeak}=V_{C1}+V_{C2}=\frac{T}{T_1-T_O}, V_{i}=\frac{1}{1-2\frac{T_0}{T}}V_{i}=BV_{i} \quad (11)$$

Where, B is the boost factor of the qZSI. This is also the peak voltage across the diode. The average current of the inductor L_1, L_2 can be calculated by the system power rating P

$$I_{L1}=I_{L2}=I_{i}=\frac{P}{V_{i}} \quad (12)$$

According to kirchoff's current law and from the above equation (13), we can also get that

$$I_{C1}=I_{C2}=I_{PN}-I_{L1}, I_D=2I_{L1}-I_{PN} \quad (13)$$

The voltage and current stress of the ZSI and qZSI are compared and have been shown in shown in Table II.

Table II: Voltage and Current stress in ZSI and qZSI

	$V_{L1}=V_{L2}$		V_{PN}		V_{diode}	
	T_O	T_1	T_O	T_1	T_O	T_1
ZSI	mV_{i}	$-nV_{i}$	0	BV_{i}	BV_{i}	0
qZSI	mV_{i}	$-nV_{i}$	0	BV_{i}	BV_{i}	0
	V_{C1}		V_{C2}		$\widehat{V}_{i}$	
ZSI	mV_{i}		mV_{i}		$\frac{MBV_{i}}{2}$	
qZSI	mV_{i}		nV_{i}		$\frac{MBV_{i}}{2}$	
	$I_{i}=I_{L1}=I_{L2}$		$I_{C1}=I_{C2}$		I_D	
ZSI	$\frac{P}{V_{i}}$		$I_{PN}-I_{L1}$		$2I_{L1}-I_{PN}$	
qZSI	$\frac{P}{V_{i}}$		$I_{PN}-I_{L1}$		$2I_{L1}-I_{PN}$	

Here, M is the modulation index; $\widehat{V}_{i}$ is the ac peak phase voltage; P is the system power rating. The relationships between modulation index and boost factor is given in (14).

$$m=\frac{T_1}{T_1-T_0};\ n=\frac{T_O}{T_1-T_O};\ \text{thus} m>1;\ m-n=1;$$

$$B=\frac{T}{T_1-T_O},\ \text{thus m + n = B, } 1<m<B. \tag{14}$$

From table II, we can find that the qZSI inherits all the advantages of the ZSI. It can buck or boost a voltage with a given boost factor. It is able to handle a shoot-through state, and therefore it is more reliable than the traditional VSI. There are some unique merits of the qZSI when compared to the ZSI: The two capacitors in ZSI sustain the same high voltage; while the voltage on capacitor C_2 in qZSI is lower, which requires lower capacitor rating. The ZSI has discontinuous input current in the boost mode, while the input current of the qZSI is continuous due to the input inductor L_1, which will significantly reduce input stress. There are less EMI problems.

CCM and DCM analysis of qZSI:

Continuous conduction mode and discontinuous conduction mode affect the performance of qZSI because the circuitry of qZSI internally consists of a DC-DC voltage boost structure with capacitors and inductors present inherently. The equations governing the qZSI are valid only in continuous conduction mode. However for DCM we need to formulate the new governing equations [21]. To yield the desirable results, the CCM and DCM operations are considered in designing of qZSI. The input inductor in the qZSI buffers the source current of the qZSI network. Thus, when the input current never drops to zero during shoot-through state, the qZSI network can operate in CCM. In CCM operation input voltage stress can be minimised which is important in power electronic applications. Even if the inductance is large, with the decrease in load the converters enter into DCM mode. In other words the converter transits from DCM to CCM or vice-versa under large load change.

Operation analysis in CCM:

The CCM operating state of the qZSI in one switching cycle consists of shoot-through state and non-shoot-through state.

$$T=D_0+D_1$$

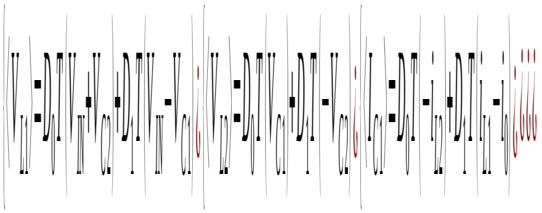
Where, D_0 represents shoot-through duty ratio and D_1 represents non-shoot- through duty ratio. A first order differential equation is obtained through the circuit analysis on the equivalent circuit of qZSI in shoot-through state shown in Fig.2 (c).The state space equation in matrix form is given by (15).

$$\begin{bmatrix} L_1 & 0 & 0 & 0 \\ 0 & L_2 & 0 & 0 \\ 0 & 0 & C_1 & 0 \\ 0 & 0 & 0 & C_2 \end{bmatrix} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_{C1}(t) \\ v_{C2}(t) \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 \\ 0 & -1 & 0 & 0 \\ -1 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_{C1}(t) \\ v_{C2}(t) \end{bmatrix} + \begin{bmatrix} 1 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} v_{in}(t) \\ i_0(t) \end{bmatrix} \tag{15}$$

Where i_{L1} is the inductor-1 current, i_{L2} is inductor-2 current, inductor -1 voltage v_{L1}, inductor-2 voltage v_{L2}, capacitor-1 current i_{C1} and capacitor-2 current i_{C2}, input voltage V_{in} and output dc current I_0. In shoot-through state DC link voltage, $V_{dc}= 0$. Now from circuit analysis of non-shoot-through state shown in Fig.2 (b), we get the expression as shown in (16) [22-23].

$$\begin{bmatrix} L_1 & 0 & 0 & 0 \\ 0 & L_2 & 0 & 0 \\ 0 & 0 & C_1 & 0 \\ 0 & 0 & 0 & C_2 \end{bmatrix} \begin{bmatrix} \dot{i}_{L1}(t) \\ \dot{i}_{L2}(t) \\ \dot{v}_{C1}(t) \\ \dot{v}_{C2}(t) \end{bmatrix} = \begin{bmatrix} 0 & 0 & -1 & 0 \\ 0 & 0 & 0 & -1 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_{C1}(t) \\ v_{C2}(t) \end{bmatrix} + \begin{bmatrix} 1 & 0 \\ 0 & 0 \\ 0 & -1 \\ 0 & -1 \end{bmatrix} \begin{bmatrix} v_{in}(t) \\ i_0(t) \end{bmatrix} \quad (16)$$

In non-shoot-through state $V_{dc}=V_{c1}+V_{c2}$. We know that the inductor current and the capacitor voltage cannot change instantaneously. Hence, in steady-state condition, the average voltage across the inductor and the average current flowing through the capacitor in one switching cycle are equal to zero. The average values are given by (17).



(17)

We obtain the steady state inductor current relationship, the input voltage and the capacitor voltages and DC-link voltages with respect to D_0 by equating our above equations to zero and thus we obtain the (18).

$$\Delta I_{L1} \quad (18)$$

Here, P is the power input of qZSI and R is the load resistance. The inductor voltages have been analyzed before. We know the current through an inductor lacks the capability of changing instantaneously. Because of this the shoot-through characteristics impart ripple effect in the inductor current. We for analysis have assumed for our system to be in steady state, increase in ripple current that happens in shoot-through state is shown as positive and is equal to decrease in ripple current in non-shoot through state which is negative. On assuming $L_1=L_2$ and f_s is the switching frequency, ΔI_{L1} and ΔI_{L2} are obtained as (19) and (20) respectively. The voltage across inductors and current through inductors for boundary cases has been shown in Fig (3).

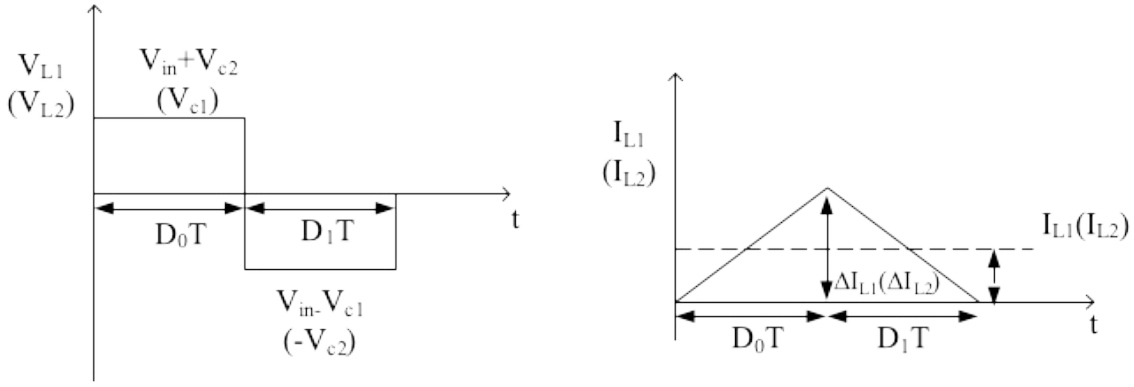


Fig. 3. *Inductor Voltage and Inductor current waveforms at boundary conditions*

$$\Delta I_{L1}=\frac{1}{L}\int_{0}^{t_0=D_0T} V_{L1}\,dt=\frac{1}{L}\int_{t_1=D_OT}^{T} V_{L1}\,dt$$

$$\Delta I_{L1}=\frac{\left(V_{in}+V_{C2}\right)\left(D_O\right)}{Lf_s} \tag{19}$$

$$\Delta I_{L2}=\frac{1}{L}\int_{0}^{t_0=D_0T} V_{L2}\,dt=\frac{1}{L}\int_{t_1=D_OT}^{T} V_{L2}\,dt$$

$$\Delta I_{L2}=\frac{\left(V_{C1}\right)\left(D_O\right)}{Lf_s} \tag{20}$$

Our boundary inductor current is half times the ripple current as given below,

$$I_{LB}=\frac{1}{2}\Delta I_L$$

The boundary currents for both the inductors will be given by (21).

$$I_{LB1}=I_{LB2}=\frac{\left(V_{in}+V_{C2}\right)\left(D_O\right)}{2Lf_s}=\frac{\left(V_{C1}\right)\left(D_O\right)}{2Lf_s} \tag{21}$$

For the proposed in continuous conduction mode, $I_L \geq I_{LB}$, for the proposed inverter to work in DCM $I_L < I_{LB}$, Therefore the condition can be established as given in (22) and (23) respectively.

$$I_{LB}\geq\frac{\left(V_{in}+V_{C2}\right)\left(D_O\right)}{2Lf_s}\,or\,\frac{\left(V_{C1}\right)\left(D_O\right)}{2Lf_s} \tag{22}$$

$$L\geq\frac{\left(V_{in}+V_{C2}\right)\left(D_O\right)}{2I_{LB}f_s}\,or\,\frac{\left(V_{C1}\right)\left(D_O\right)}{2I_{LB}f_s} \tag{23}$$

Therefore for a known inductance minimum inductor current before DCM starts will be given by (24).

$$I_{LB\min}=\frac{\left(V_{in}+V_{C2}\right)\left(D_O\right)}{2Lf_s}\,or\,\frac{\left(V_{C1}\right)\left(D_O\right)}{2Lf_s} \tag{24}$$

DCM operation analysis:

In DCM the steady- state voltage conversion equation used earlier does not hold. For analysis we need to use inductor waveform of DCM. The inductor current thus obtained will be given by (25)

$$I_L=\frac{1}{2}\times\frac{1}{T}\times\Delta I_L\times\left(D_OT+\frac{V_{in}+V_{C2}}{V_{in}-V_{C1}}D_OT\right) \tag{25}$$

By performing substitutions we obtain the voltage ratio as given in (26).

$$\frac{V_{dc}}{V_{in}}=\frac{D_O}{1-D_O}\sqrt{\frac{R(D_O-1)}{2Lf_s(D_O)}} \tag{26}$$

the above analysis it is inferred that in DCM , the voltage conversion ratio is a function of $V_{¿}{}'D_O$,L and After
R. Thus the transition from CCM to DCM depends on load and resistance.

Below given are the output current and voltage equations,

$$V_{Orms}=\frac{MV_{dc}}{\sqrt{2}}$$

$$I_{Orms}=\frac{I_{Opeak}}{\sqrt{2}}$$

for M=1;

$$\frac{Lf_sI_O}{V_{in}}=D-D^2$$

$$V_{in}=2\frac{\hat{V}_{in}}{M}$$

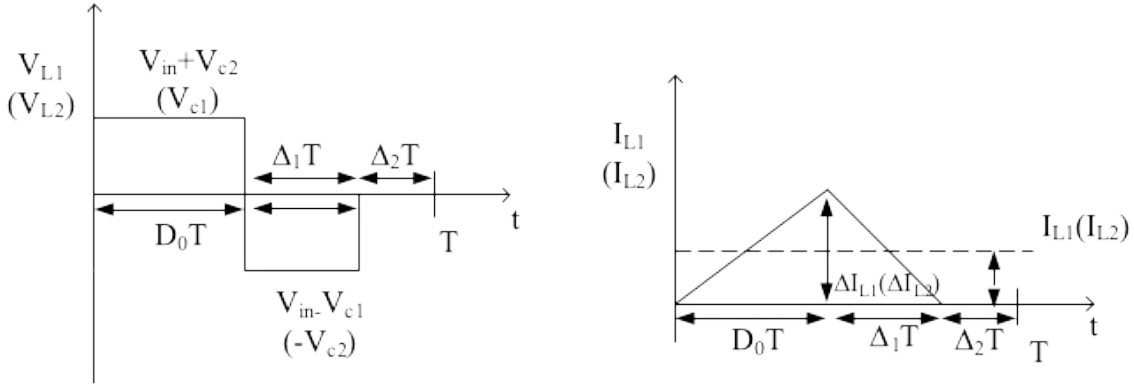


Fig. 4. *Inductor Voltage and current waveforms for discontinuous conduction mode*

$$150=2\frac{\hat{V}_{in}}{0.9}$$

$$\hat{V}_{in}=67.5V$$

Where the minimum value of input voltage is 150V

$$G=\frac{M}{\sqrt{3}M-1}=\frac{0.9}{(\sqrt{3}\times 0.9)-1}=1.61$$

$$M_{\min}=\frac{G_{\max}}{\sqrt{3}G_{\max}-1}=\frac{1.61}{\sqrt{3}(1.61)-1}\approx 0.9$$

$$B_{\max}=\frac{1}{\sqrt{3}M_{\min}-1}=\frac{1}{\sqrt{3}(0.9)-1}\approx 1.78$$

$$\hat{V}_{PN}=B_{\max}V_{in}$$

$$\hat{V}_{PN}\approx 267\,V$$

Thus maximum voltage stress on Inverter Bridge is predicted to be 267V. Let the system be of power rating 1KW.

$$I_{in}=I_{L1}=I_{L2}=\frac{P}{V_{in}}=\frac{1\times 10^{3}}{150}=6.67\,A$$

I_{in} is maximum current flowing in an inductor. The inductor voltage and current waveforms for discontinuous conduction mode are shown in Fig. (4).

Inductor and capacitor selection:

When the qZSI inverter works in the boost conversion mode, the potential maximum interval of the shoot-through state is calculated as:

$$T_{0\max}=\frac{2-\sqrt{3}M_{\min}}{f_s}=\frac{2-\sqrt{3}(0.9)}{20\times 10^{3}}\approx 2.2\,ms$$

If Peak to peak ripple $r_c\%$ is having value as 20% for the proposed system, the inductance can be calculated as:

$$L_1=L_2=\frac{V_L\Delta T}{\Delta I}=\frac{mV_{in}}{I_{L\max}r_c\%}\cdot\frac{1}{2}T_{0-\max}$$

From the observations done earlier, capacitor voltageC_1 is 250V. Therfore,

$$mV_{in}=V_{C1}$$

$$m(150)=250$$

$$m=1.66$$

$$L_1=L_2=\frac{1.66\times 150}{6.67\times 0.2}\times\frac{1}{2}\times 2.2\times 10^{-3}\approx 2.05\times 10^{-3}\approx 2.05\,mH$$

The capacitance of two capacitors is:

$$C_1=C_2=\frac{2.I_L\Delta T}{\Delta(V_{C1}+V_{C2})}=2\cdot\frac{I_L}{BV_{in}r_v\%}\cdot\frac{1}{2}T_{0-\max}$$

Where $r_v\%$ =0.017 (assumed). The capacitance of two capacitors is:

$$\Rightarrow C_1=C_2=2\cdot\frac{6.67}{1.78\times 150\times 0.017}\times\frac{1}{2}\times 2.2\times 10^{-3}\approx 646.5\,\mu F$$

$$L_1=L_2\approx 2.05\,mH$$

Thus,

$$C_1=C_2\approx 646.5\,\mu F$$

3. Experimental setup and Hardware Results

The hardware setup of the proposed system is developed to obtain the practical results and all the components have been shown in Fig. (5). For proof of the proposed concept, the actual panels have been replaced with dc link voltages and battery system by a resistive load. The dspic microcontroller board (PIC16F877A) have been used to generate PWM signal. The dspic signal is provided to gate drives circuit which isolates and amplifies

the signals to a suitable value for turning ON the semiconductor switches. The PWM signals with proper shoot through states and non shoot through states has been shown in (6).

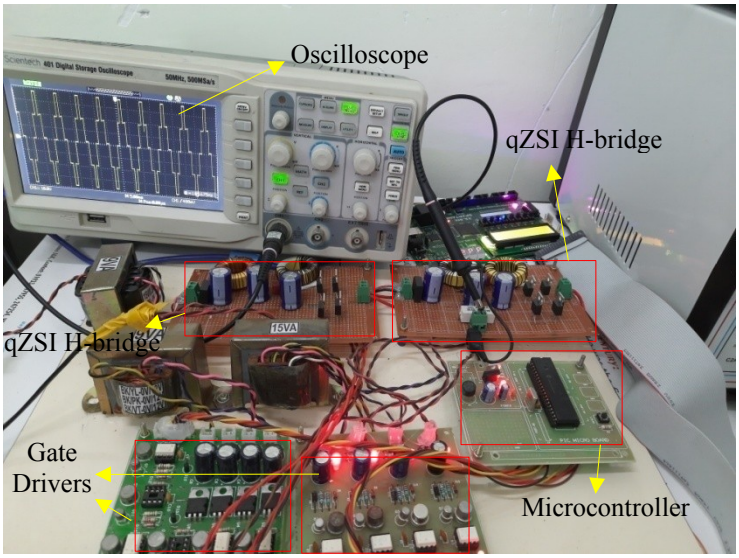


Fig.5 Hardware setup

The low frequency control is obtained based on the mathematical model developed in the paper. The gating signals for individual cells are shown in (6). The stable operation is ensured by adjusting the gain of the controller. The proposed scheme has been implemented in grid connection mode and the complete schematic has been shown in (7). In the proposed scheme, the injected current into the grid is confirmed at unity power factor and the harmonics content in it is minimum. For this purpose there is only β-component of the current (*sinωt*) and thus α- component is created for necessary-

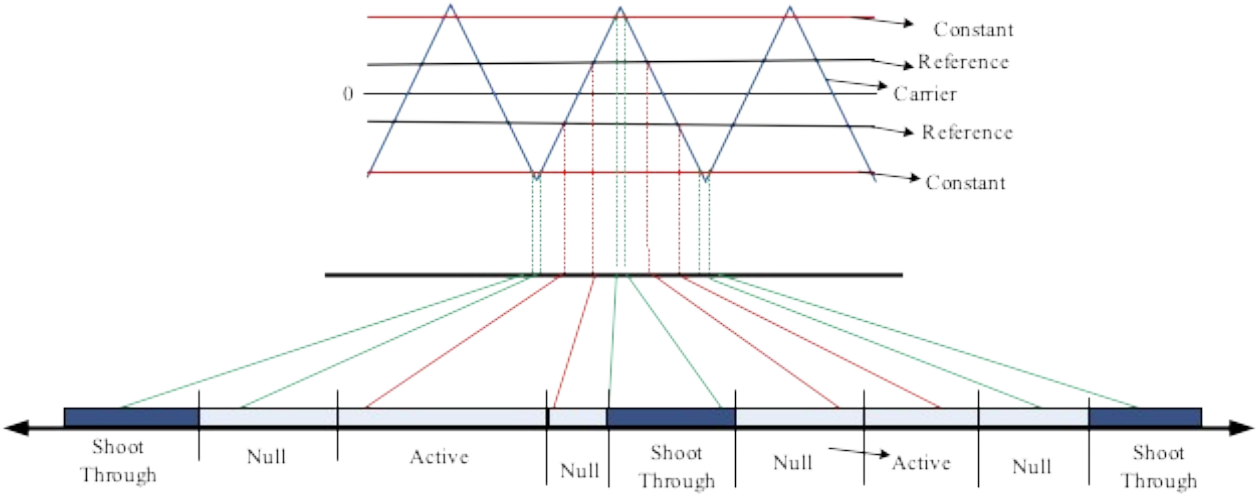


Fig.6 PWM signal with shoot through and non shoot through states

transformations. The transformation into d-q coordinates results into dc component. The required ρ angle is chosen between αβ and d-q co-ordinates axes. In order to keep $v_q^*=0$, the ρ is taken in such a way that *dq*-axis is aligned along the v_d. Therefore, the $v_\alpha^*$and v_β^* will work as reference and it is compared with a triangular signal and based on the logic the PWM pulses are generated. The shoot through reference line is adjusted so that the required boost is obtained at the output.

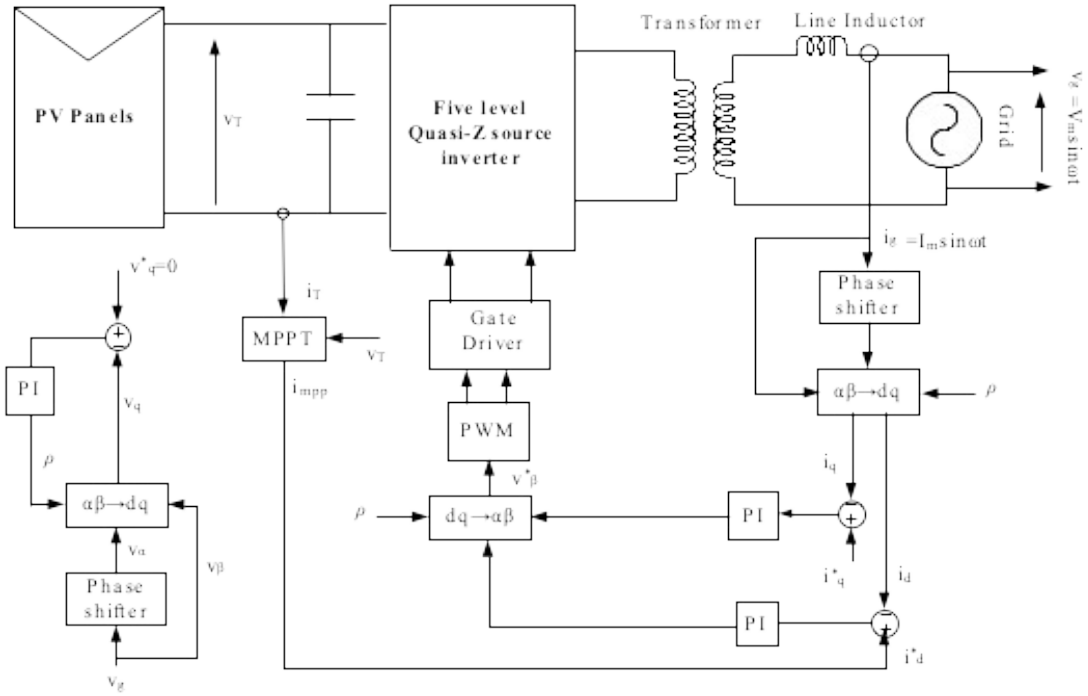


Fig.7 Control system design

Table III: Voltage and Current stress in ZSI and qZSI

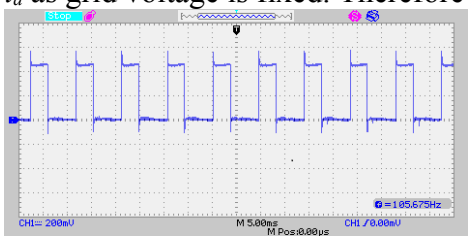
```
#include<pic.h>
#include<stdio.h>
#define _XTAL_FREQ 10000000
__CONFIG(0x3f72);
void main()
{
        TRISC=0x00;
        PORTC=0;

        while(1)
        {
                        PORTC=0xcc;
                __delay_ms(2);

            PORTC=0xc9;
                __delay_ms(2);

                PORTC=0x99;
                __delay_ms(2);

        PORTC=0xc9;
                __delay_ms(2);

                PORTC=0xcc;
                __delay_ms(2);
                PORTC=0x36;
                __delay_ms(2);
      PORTC=0x66;
```

```
                __delay_ms(2);
                PORTC=0x36;
                __delay_ms(2);

//              PORTC=0x33;
//              __delay_ms(2);

        }
}
```

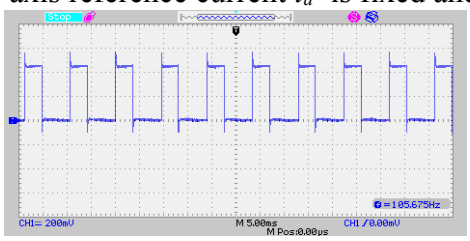
Table III: Voltage and Current stress in ZSI and qZSI

Dspic	PIN	Switces	Inverter bridge
RC0	15	1	H-bridge-1
RC1	16	2	
RC2	17	3	
RC3	18	4	
RC4	23	5	H-bridge-2
RC5	24	6	
RC6	25	7	
RC7	26	8	

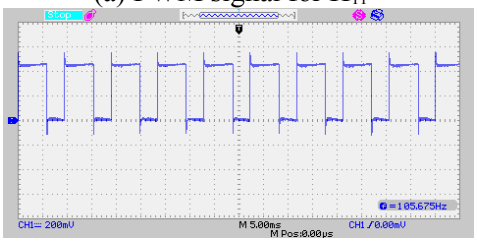
only v_β^* component is required in this case as v_β and i_β are already known and v_β^* component is calculated. Here the PV generated power pumped into the grid will be proportional to the current d-axis current i_d as grid voltage is fixed. Therefore the d-axis reference current i_d^* is fixed and it is



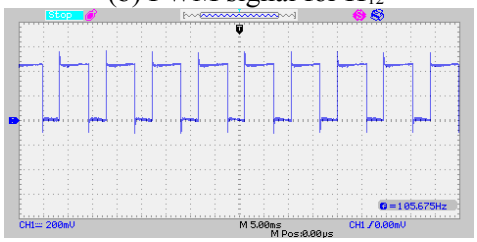
(a) PWM signal for H_{11}



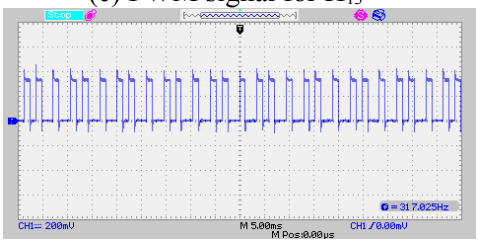
(b) PWM signal for H_{12}



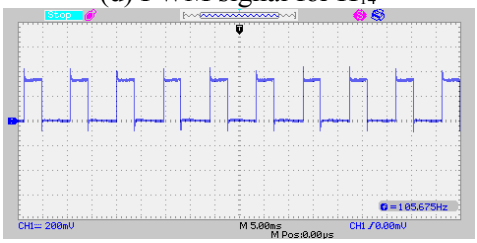
(c) PWM signal for H_{13}



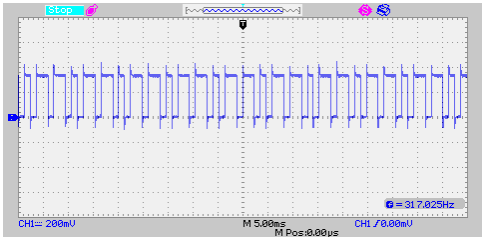
(d) PWM signal for H_{14}



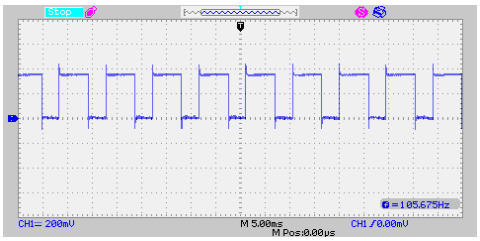
(e) PWM signal for H_{21}



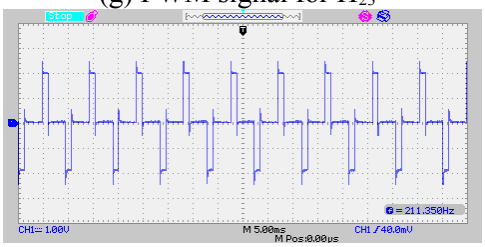
(f) PWM signal for H_{22}



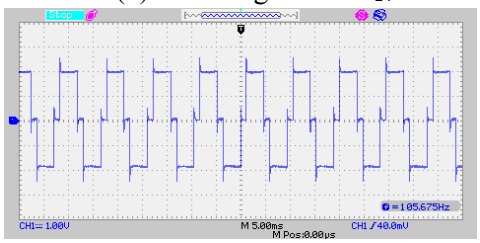
(g) PWM signal for H_{23}



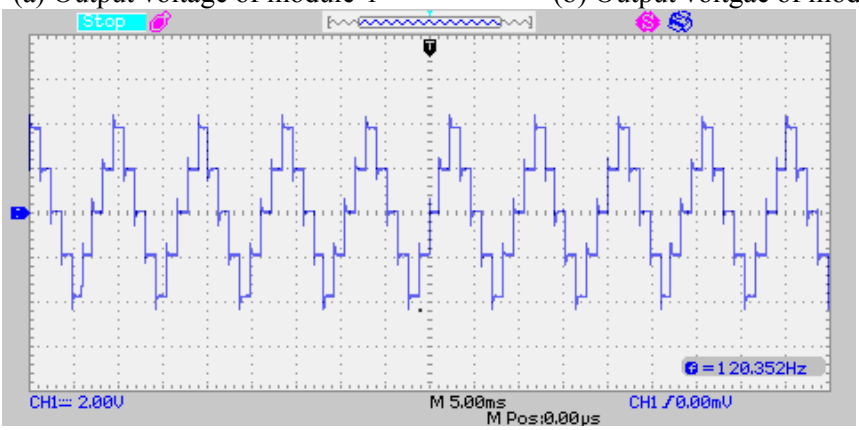
(h) PWM signal for H_{24}



(a) Output voltage of module-1



(b) Output voltgae of module-2



(i) Multilevel output voltage

Fig.8 Output gate pulses, module output and multilevel output voltage

obtained from the MPPT algorithm. So i_d^* is nothing but the output current from the MPPT algorithm and it will try to track the d-axis current i_d. The main programme for generating PWM pulses in dspic microcontroller is shown in Table 2. The Pin numbers in for generating all the eight PWM pulses is shown in Table 3. The PWM pulses, H-bridge module outputs and the output voltage of five level quasi Z-source inverter is shown in table-III. The gate pulses to various semiconductor switches, module output voltage and multilevel output voltage have been shown in Fig. 8(a) to Fig. 8(i) respectively. The hardware results validate the proposed concept in this paper.

4. Conclusion

In this paper a novel microcontroller based low switching frequency based pulse width modulation technique for multilevel quasi Z source inverter has been investigated and implemented. The component design of quasi z source inverter (qZSI) is first considered with continuous and discontinuous mode of operations. The detailed modelling for qZSI is then established for effective implementation of PIC microcontroller (PIC 16F877A) for generating the PWM pulses. The prototype of five level quasi z-source inverter by having two H-bridge modules have been developed and PWM signals have been applied by suitably adjusting the shoot through and non shoot through switching states. The computational and hardware result shows the effective implementation of the proposed scheme.

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