

ARTICLE TYPE

Comparison of Low-Frequency-Commutation Modulation Techniques in a Symmetrical Cascaded H-Bridge Multilevel Inverter

Juan H. Almazán Covarrubias¹ | Pedro M. García Vite^{*1} | Juan M. Ramírez Arredondo²

¹DEPI, Tecnológico Nacional de México/Instituto Tecnológico de Cd. Madero, Tamaulipas, Mexico

²SEP, Centro de Investigación y de Estudios Avanzados del I.P.N., Jalisco, México

Correspondence

*Pedro Martín García Vite. Email: pedro.gv@cdmadero.tecnm.mx

Present Address

Primero de Mayo con Sor Juana Inés de la Cruz s/n, Los Mangos 89440

Summary

Among the power inverters, modular multilevel converters (MMC) have gained popularity due to their advantages over conventional two-level inverters. Although the MMC utilizes more power switches than traditional inverters, the former exhibits notable benefits such as low total harmonic distortion, low switching losses with lower voltage stress, high power quality, reduced electromagnetic interface, and modularity with numerous degrees of freedom to synthesize output waveforms. Concerning the synthesized voltage quality, several low-frequency modulation techniques have been proposed to produce output voltage with low harmonic content. A particular case of study consisting of a three-phase even-level MMC inverter is taken as a benchmark to comparatively evaluate four methods for synthesizing high-quality output voltage. The employed techniques are (i) selective harmonic elimination (SHE), (ii) generalized SHE, (iii) THD Voltage Minimization, and (iv) Optimum Nearest Level Modulation, selected based on the phase and line-to-line output voltage THD. The model is formulated to compute the commutating angles to control the MMC submodules. Simulations show individual performance under the same operating conditions. A lab-scale prototype is built to corroborate the theoretical approach. The results allow the selection of the most convenient modulation technique based on the number of commutations and harmonic spectrum.

KEYWORDS:

Modulation techniques, modular multilevel converter, selective harmonic elimination, total harmonic distortion

1 | INTRODUCTION

Power electronics converters cover various applications, from portable devices of a few watts to power transmission and conditioning to several megawatts. At a low power level in the midway, some applications require dc-to-ac conversion. In such a case, the fundamental component of the output voltage can be extracted through an LC low-pass filter when the SPWM technique is employed to control an H-bridge in two- or three-level inverter. However, switching losses on semiconductors become significant for high-power applications: MOSFET is limited by its ratings and IGBTs by its commutation speed. To address this

⁰**Abbreviations:** THD, total harmonic distortion; MMC, modular multilevel converter; PWM, pulse width modulation, SHE, selective harmonic distortion; GSHE, generalized SHE; vTHDmin, voltage THD minimization; ONLM, optimum nearest level modulation.

inconvenience, multilevel inverter (MLI) topologies have been proposed¹. MLI has become a mature technology, especially the voltage-fed type¹. The MLI has become an essential alternative among these topologies since it possesses numerous advantages compared to traditional two- and three-level structures. The most remarkable benefits are lower harmonic content in the output voltage and current, better electromagnetic compatibility, and reduced switching losses with low stress on switch devices^{2,3}. Due to the mentioned advantages, MLIs have excelled in multiple applications, such as reactive power compensation¹, energy storage systems⁴, flexible ac transmission systems (FACTS), and renewable energy conversion^{5,6}. MLI structures can be classified as diode-clamped MLI, flying capacitor MLI, and cascaded H-bridge (CHB) MLI¹. Due to its modularity, the latter can be easily extended, producing a more sinusoidal-type waveform with low THD. However, as the number of modules increases, the circuitry complexity and the semiconductor power losses also increase. Several commutation strategies have been proposed to guarantee a low-order harmonic content at the output but employ a limited number of levels so that the disadvantages mentioned above are attenuated^{5,7,8,9,10}. Regarding these strategies, modulation techniques control semiconductors' conduction and blocking times based on a particular target, such as reduced input current ripple, low THD, and/or specific voltage⁹. Selective harmonic elimination is founded in the Fourier analysis and first appeared in a single-phase inverter application¹¹. Thus, four of the most employed strategies are (i) the selective harmonic elimination (SHE), (ii) generalized (gSHE), (iii) THD Voltage Minimization (vTHDmin), and (iv) Optimum Nearest Level Modulation (ONLM), which are employed to control a three-phase seven-level based on cascaded H-bridge modular configuration. The four strategies are deeply analyzed and compared using low-frequency modulation techniques. Considering the order and amplitude of the harmonic components, it is worth mentioning that the harmonic spectrum will define the most convenient modulation technique. This work aims to analyze and compare, through experimental tests and the simulation, the low-frequency modulation techniques effects on the synthesized voltage of a seven-level CHB-MLI. Then, the harmonic spectrum of the output waveform is proposed to evaluate the performance of each modulation technique. The rest of the paper is organized as follows: Section 2 provides a brief review of the symmetrical cascaded H-bridge multilevel inverter is performed, where a general classification is given to identify the case study. In Section 3, the four low-frequency modulations (SHE, gSHE, vTHDmin, and ONLM) are studied in depth, including the procedures to compute the commutation angles for the case study. Then, in Section 4 the obtained commutation angles are employed to control the MLI, followed by the verification and measurement of the phase and line-to-line output voltage. These results are corroborated via prototype, which is detailed in Section 5. The most relevant features are compared and discussed in Section 6. Finally, the conclusion closes the paper, in Section 7.

2 | THREE-PHASE CASCADED MULTILEVEL INVERTER (MLI)

Voltage source inverters can be classified from different points of view¹². Regarding the number of levels the output voltage can achieve, voltage source converters are classified as two-level or multilevel inverters. Single or multiple sources can feed MLIs. For MLI configurations, half- or full-bridge submodules can be constituted by symmetric or asymmetric voltage sources. The topology proposed by Sedaghati and Latifi is an example of multiple sources configuring as symmetrical or asymmetrical, generating up to twenty-one levels³. A general classification can be seen in Figure 1. This study is focused on a symmetric-voltage-fed seven-level HB-MLI; nonetheless, the methodology can be applied to other topologies. The asymmetric configuration facilitates using hybrid topologies, allowing nested configurations such as E-type and ST-type, have been proposed^{13,14}. Those hybrid configurations employ low-stress four-quadrant power switches though¹⁵. Besides, hybrid topologies allow implementing of various algorithms, achieving particular objectives¹⁶, with a reduced number of switches, such as the configuration proposed by Anand and Singh that uses eleven switches and three sources suited for PV application.

Due to its stackable and modular configuration, the cascaded multilevel inverter has been applied in various industrial applications at high voltage levels. Independently on the type of source configuration, each SM handles a fraction of the total voltage.

Figure 2 shows the configuration under study composed of “s” HB cascaded-connected SMs corresponding to each “x” phase. Each SM is fed by a $V_{(x,j)}$ DC source, with $j = 1, 2, \dots, s$. The values v_{aN} , v_{bN} and v_{cN} constitute the phase voltages whereas v_{ab} , v_{bc} , and v_{ca} are the line-to-line voltages.

Figure 3 contains the various representation of the SM constitution. In Figure 3.a the general block is illustrated by a commonly used diode-transistor symbol for representing the SM, in Figure 3.b the conceptual function represented by one single-pole double-throw switch (SPDT) for each output terminal of the SM is shown. Figure 3.c illustrates the switch realization with semiconductors. The output voltage of each SM v_{xy} is obtained by controlling the position of switches sw_1 and sw_2 with a

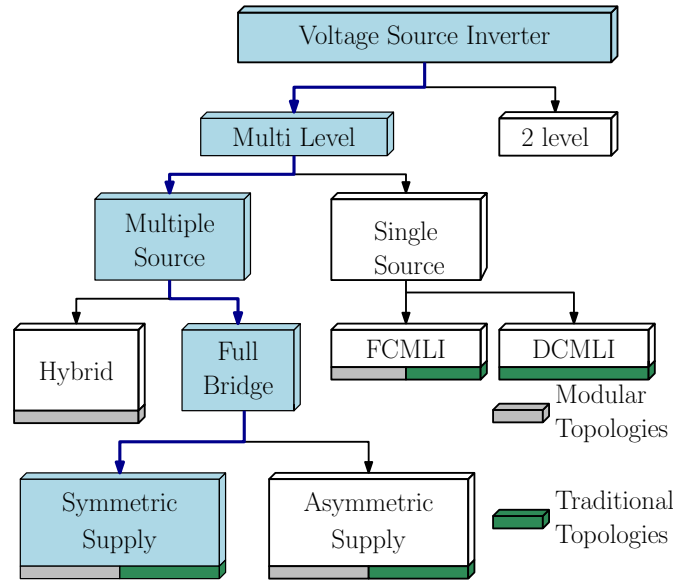


Figure 1 Most commonly voltage source inverters classification. A symmetric waveform is synthesized by means of HB submodules fed by individual DC sources.

switching function “ S ”, resulting in four commanding signals ($q_{x,k}$, with $k = 1, 2$). Since only one control signal is required for controlling the SPDT switch, the signals on transistors are complementary to each other in each leg of the SM.

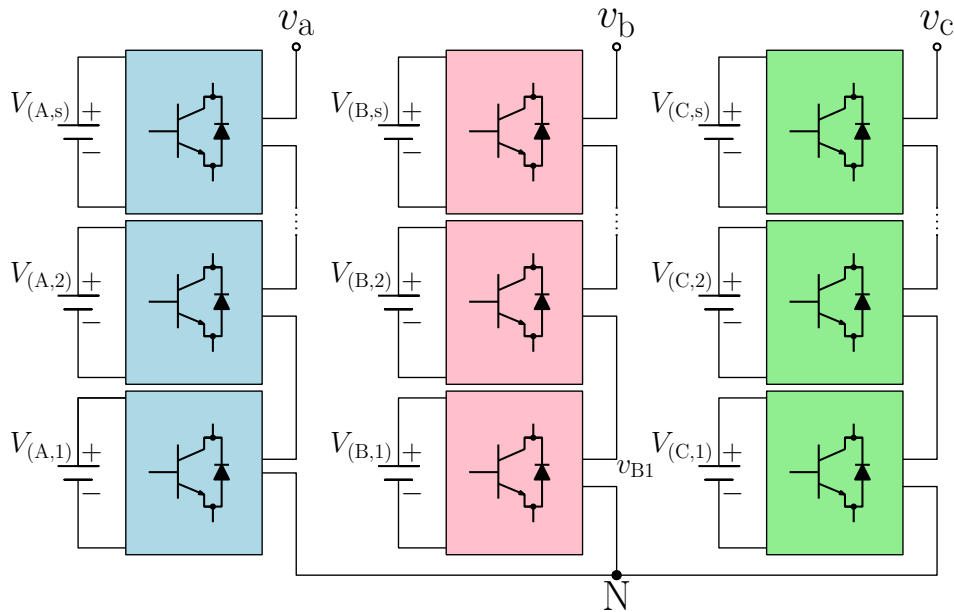


Figure 2 Three-phase cascaded multilevel inverter of “I” levels.

Thus, the value of “ S ” determines the actual position according to:

$$S_{x,k} = \begin{cases} 0, & \text{if } P \rightarrow T_1 \\ 1, & \text{if } P \rightarrow T_2 \end{cases} \quad (1)$$

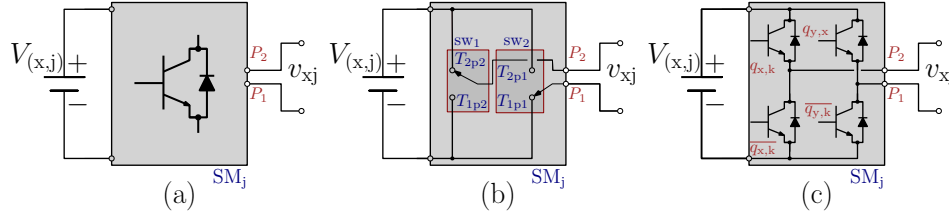


Figure 3 Different representation of the SM, belonging to the phase x and position j : (a) generic symbol, (b) SM conforms by two conceptual SPDT switches, and (c) semiconductors realization of the SPDT switches.

where “ x ” represents the phase and “ k ” stands for each power switch and “ \rightarrow ” stands for the connection of the pole (P) to the corresponding throw (T)¹⁷.

Given the symmetric nature of the CHB multilevel inverter, DC sources possess the same magnitude, allowing to synthesize levels of the same values. Then, a simplification can be made as:

$$V_{DC} = V_{(x,1)} = V_{(x,2)} = \dots = V_{(x,s-1)} = V_{(x,s)}. \quad (2)$$

Therefore, the number of levels per phase (L_{ph}) and the number of level line-to-line (m) are given by (3a) and (3b), respectively.

$$L_{ph} = 2s + 1, \quad (3a)$$

$$m = 2L_{ph} - 1. \quad (3b)$$

Finally, for a symmetric CHB-MLI with three DC sources per phase ($s = 3$) the number of levels is seven, being controlled by $N_{(sw)} = 2 \cdot s = 6$ switching functions.

Under this consideration, the phase voltage can be determined by the switching functions, according to:

$$v_{xN} = V_{DC} \sum_{k=0}^{l-1} [S_{x,(2k+1)} - S_{x,(2k+2)}] \quad (4)$$

3 | LOW FREQUENCY MODULATION TECHNIQUES

Modulation techniques are implemented to control the ON–OFF state of the MLI power switch devices. Unlike multicarrier modulation techniques, low-frequency modulation techniques allow for synthesizing a desired fundamental output voltage while keeping the commutations low. Thus, the commutation loss is reduced. Therefore, using a suitable modulation technique helps to improve the efficiency of the inverter^{18,19,20,21,22}. The output voltage is a staircase waveform obtained by adding the independent DC sources, Figure 4 illustrates this idea. For the case of pure staircase generation waveform in Figure 4(b) and the generation of staircase-type output voltage containing notches in Figure 4(c). The same power stage is controlled by commanding signals $q_{A,(1\sim6)}$ with different patterns. For the case of Figure 4(b) three symmetrically distributed angles are employed ($\alpha_{1\sim3}$), whereas the scheme in Figure 4(c) employs up to nine angles ($\alpha_{1\sim9}$).

The switching low-frequency modulation can be classified as harmonic elimination and minimization/optimization techniques. The most used for harmonic elimination are quarter- and half-wave symmetry, nonsymmetrical and unequal with variable levels. For the optimization techniques, the most remarkable become harmonics minimization, THD minimization, harmonic mitigation, and optimum nearest level. It is worth mentioning that, in the cascaded multilevel inverters, low-frequency modulation techniques have the particularity of controlling the number of commutations per cell, thus diminishing the losses caused by the power switches. However, the harmonic content exceeds 5%, which may not be entirely suitable for devices interconnected to the inverter. In this work, the Selective Harmonic Elimination (SHE), Generalized Selective Harmonic Elimination (GSHE), Voltage THD Minimization (vTHD_{min}), and Optimum Nearest Level Modulation techniques are deeply analyzed and compared.

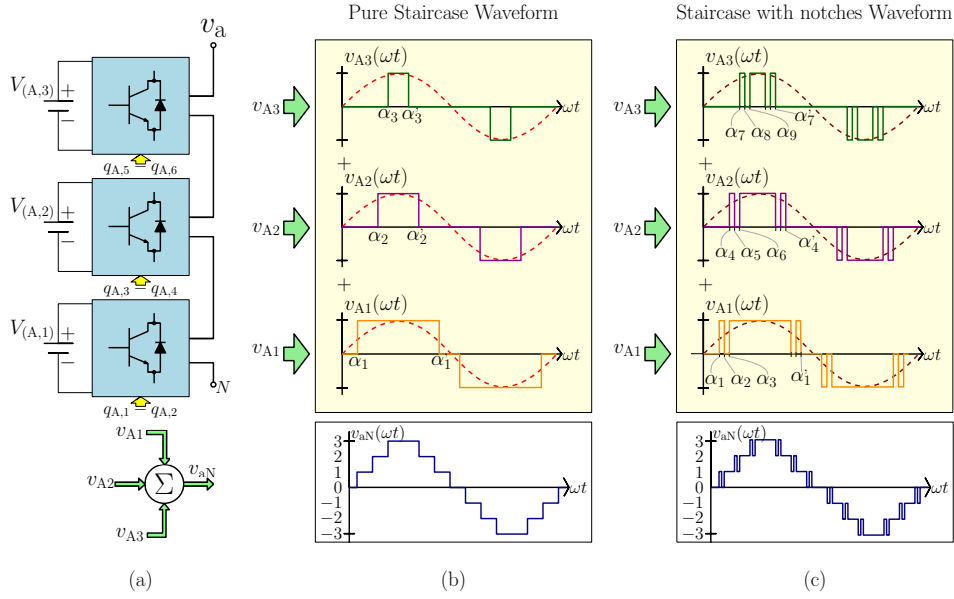


Figure 4 General implementation schemes for reduced low-order harmonic content: (a) synthesis of v_{aN} voltage out of independent DC sources ($V_{A,1} - V_{A,3}$), (b) pure staircase waveform manipulated by three angles, and (c) staircase waveform containing notches controlled by nine angles.

3.1 | Selective Harmonic Elimination

The Selective Harmonic Elimination (SHE) technique was first proposed in 1964 to control a single-phase inverter¹¹, it has been successfully applied to numerous configurations in symmetric and asymmetric schemes²³. Notably, in a seven-level inverter, the SHE technique generates a fundamental sine voltage waveform with three commutation angles: α_1 , α_2 , and α_3 , following that $\alpha_1 < \alpha_2 < \alpha_3$. These angles are employed to synthesize an output voltage. The critical process eliminates undesired harmonics, allowing a previously established modulation index to control the fundamental component. Figure 5 shows a seven-level waveform $f(\omega t)$ in its fundamental form. The amplitude has been normalized to V_{DC} per level, with the peak value equal to $3V_{DC}$.

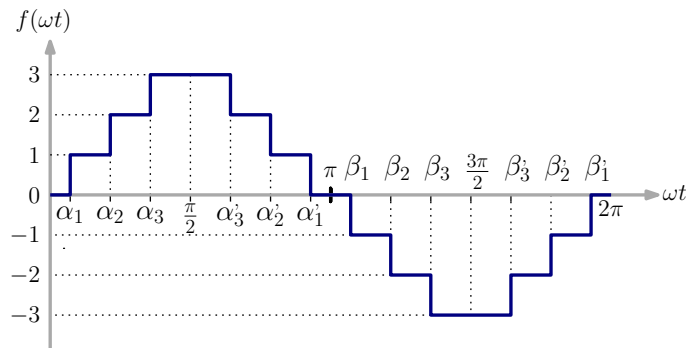


Figure 5 Seven-level waveform in its fundamental form. Notice that the angles α_i are mirrored respect to the $\pi/2$ and $3\pi/2$ values.

In Figure 5, the angles $\alpha'_i = \pi - \alpha_i$ with $i = 1, 2, 3$ have been introduced to avoid notational clutter. Similarly, for the negative semicycle β angles are introduced as $\beta_i = \alpha_i + \pi$ and $\beta'_i = 2\pi - \beta_i$. The complete set of angles can be described as:

$$\begin{aligned}\alpha'_1 &= \pi - \alpha_1; \beta'_1 = \pi + \alpha_1; \beta'_1 = 2\pi - \beta_1; \\ \alpha'_2 &= \pi - \alpha_2; \beta'_2 = \pi + \alpha_2; \beta'_2 = 2\pi - \beta_2; \\ \alpha'_3 &= \pi - \alpha_3; \beta'_3 = \pi + \alpha_3; \beta'_3 = 2\pi - \beta_3.\end{aligned}$$

Following this angle's relationship, a symmetrical distribution around $3\pi/2$ is obtained. In this case, the fifth and seventh harmonics are selected to be eliminated for a seven-level-CHB MLI. When applying the Fourier analysis theory to the output voltage, a set of nonlinear equations must be solved for the unknown angles of each quarter cycle of the fundamental. The Fourier series expansion of the output voltage waveform can be defined as follows:

$$f(\omega t) = \frac{A_0}{2} + \sum_{n=1}^{\infty} [A_n \cos(n\omega t) + B_n \sin(n\omega t)] \quad (5)$$

where $\omega = 2\pi/T$.

Due to the nature of the waveform and the quarter wave (QW) symmetry, the DC component A_0 and the Fourier coefficient A_n are both equal to zero. Therefore, (5) can be rewritten as follows :

$$f(\omega t) = \sum_{n=1}^{\infty} b_n \sin(n\omega t) \quad (6)$$

where the b_n coefficients are calculated by means of:

$$\begin{aligned}b_{2n} &= 0, \\ b_{2n-1} &= \frac{8}{2\pi} \int_0^{\frac{\pi}{2}} f(\omega t) \sin(n\omega t) d(\omega t).\end{aligned}$$

Then, the set of nonlinear trigonometrical equations, corresponding to the fundamental, third, and fifth harmonics that correctly eliminates the undesirable harmonics for a seven-level CHB-MLI can be formulated. This set includes a modulation index m_i and is a function of the three angles α_i as shown below:

$$\begin{aligned}f_1(\alpha_1, \alpha_2, \alpha_3) &= \sum_{x=1}^3 \cos(\alpha_x) - K = 0 \\ f_2(\alpha_1, \alpha_2, \alpha_3) &= \sum_{x=1}^3 \cos(5\alpha_x) = 0 \\ f_3(\alpha_1, \alpha_2, \alpha_3) &= \sum_{x=1}^3 \cos(7\alpha_x) = 0\end{aligned} \quad (7)$$

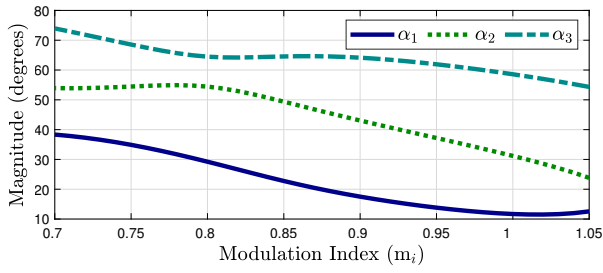
where $K = 3\pi m_i/4$ and $m_i = V_{1av}/(3V_{DC})$. The term V_{1av} represents the normalized magnitude of the fundamental component whereas $3V_{DC}$ is the peak value of the output voltage, produced when the voltage of the three DC sources are added.

Figure 6a shows the commutation angles α_1 , α_2 and α_3 , measured in electrical degrees, that satisfy (7), versus the modulation index ($0.7 < m_i < 1.05$). It is important to highlight that m_i values outside this range will generate overlapping angle values at the output waveform.

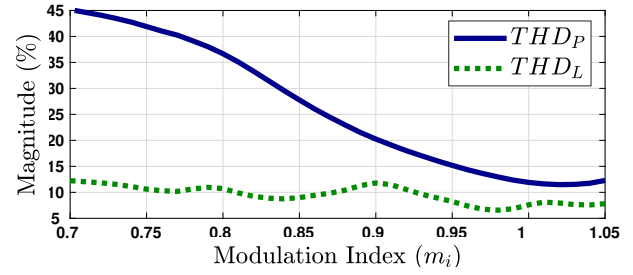
Figure 6b shows the phase (THD_p) and line-to-line (THD_L) voltage total harmonic distortion as a function of the modulation index m_i . Notice that the lowest THD values are obtained when the m_i is near to one. For the case of a unitary modulation index, ($m_i = 1$), the commutation angles are: $\alpha_1 = 11.68^\circ$, $\alpha_2 = 31.17^\circ$ and $\alpha_3 = 58.57^\circ$, as seen in Figure 6a. The solution for these angles is obtained through Matlab's Optimization Tool, which employs several methods of minimization and solution of non-linear equations.

3.2 | Generalized Selective Harmonic Elimination

Similar to the previous method, this technique calculates multiple commutation angles; however, the main difference is that to ensure a lower harmonic content, the number of angles along with their corresponding angles are increased²⁴. Figure 7 shows



(a) Commutation angles given a variable modulation index, making use of SHE close to the fundamental commutation frequency.



(b) SHE technique phase and line to line voltages THD given a variable m_i .

Figure 6 SHE modulation technique.

a seven-level voltage waveform using this modulation technique. The waveform possesses notches inserted after the original transition provided by the conventional SHE technique presented in Figure 5. Such notches add two new angles to each level, resulting in three times the number of angles in a quarter of the waveform. Besides, the angles $\alpha'_i = \pi - \alpha_i$ with $i = 1, 2, \dots, 8, 9$ have been introduced to avoid notational clutter. Similarly, for the negative semicycle the angle β is introduced as $\beta_i = \alpha_i + \pi$ and $\beta'_i = 2\pi - \beta_i$.

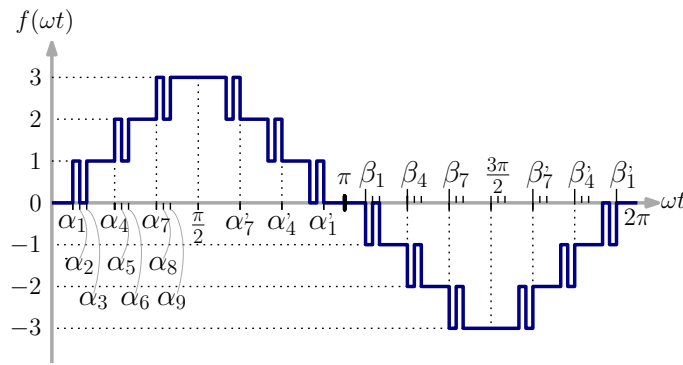


Figure 7 Seven-level voltage waveform, containing a notch which adds two new angles per level. The angles α_i are mirrored respect to the $\pi/2$ and then displaced half cycle which gives a quarter-wave symmetry.

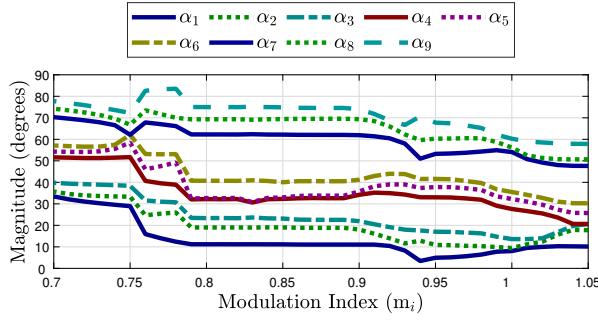
By Fourier series expressed in (5) and the QW symmetry of Figure 7, the set of equations presented in (8) must be solved in order to eliminate the corresponding harmonics.

$$f_j(\alpha_1, \dots, \alpha_9) = \sum_{x=1}^{j=9} E_{dge} \cos(h \cdot \alpha_x) - K_j = 0; \quad \text{for } j = 1, 2, \dots, 9. \quad (8)$$

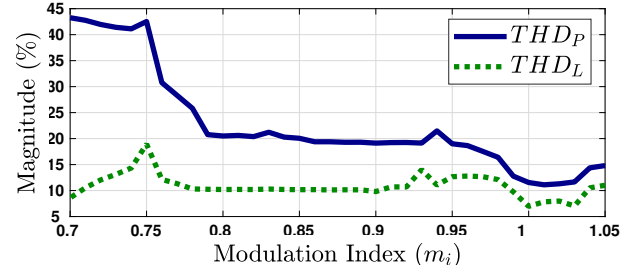
where $h = \text{int}\left(\frac{j}{2}\right) \cdot 4 + \text{int}\left(\frac{j-1}{2}\right) \cdot 2 + 1$ and $K_1 = 3\pi m_i/4$ and zero for the rest. Moreover, the operator “int” stands for the integer part of $[\cdot]$ and E_{dge} is equal to 1 or -1 in the case of rising or falling edge, respectively. For the given range of j , the values of h are 1, 5, 7, 11, 13, 17, 19, 23, 25.

Similarly to (7), (8) is also solved using the Matlab's Optimization Tool application; to obtain commutation angles α_1 to α_9 given a variable modulation index. Figure 8 shows the obtained angles and the THD of the output voltage, employing the generalized SHE technique.

Figure 8a shows the commutation angle values that satisfy (5), considering a modulation index from 0.7 to 1.05. Figure 8b shows the phase and line-to-line voltage THD given a variable m_i . Notice that the lowest THD values are obtained when m_i is close to one. For the case of a unitary modulation index, ($m_i = 1$), the commutation angles are: $\alpha_1 = 8.043^\circ$, $\alpha_2 = 9.453^\circ$, α_3



(a) Commutation angles given a variable modulation index calculated from the GSHE mathematical formulation.



(b) THD of the phase and line-to-line voltages for $0.7 < m_i < 1.05$.

Figure 8 Commutation angles and THD voltage spectrum obtained through the generalized SHE modulation technique.

$= 13.616^\circ$, $\alpha_4 = 27.610^\circ$, $\alpha_5 = 32.251^\circ$, $\alpha_6 = 35.505^\circ$, $\alpha_7 = 54.087^\circ$, $\alpha_8 = 56.202^\circ$, and $\alpha_9 = 60.278^\circ$. Such angles were found using Matlab's Optimization Tool, which employs several methods of minimization and solution of non-linear equations.

3.3 | Voltage THD Minimization

The MLI output voltage harmonic content is the parameter most often desired to be optimized. This is due the voltage is subjected to norms and standards that must be met to ensure the correct operation of the connected load^{25,26}. THD definition is given by:

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} v_n^2}}{v_1} \quad (9)$$

where v_n is the rms values of the harmonics. Considering the voltage shown in Figure 5, it is possible to relate the THD as a function of the commutation angles. The following equation shows the function to be optimized or minimized by doing these manipulations²⁶.

$$THD_{v_{aN}} = \frac{25\sqrt{2}\sqrt{9\pi^2 - A - B - C}}{\cos(\alpha_1) + \cos(\alpha_2) + \cos(\alpha_3)}, \quad (10)$$

where:

$$\begin{aligned} \alpha_1 &\leq \alpha_2 \leq \alpha_3 \leq 90^\circ \\ A &= \frac{\pi^2}{90}(\alpha_1 + 3\alpha_2 + 5\alpha_3), \\ B &= 8 [\cos^2(\alpha_1) + \cos^2(\alpha_2) + \cos^2(\alpha_3)], \\ C &= 16[\cos(\alpha_1)\cos(\alpha_2) + \cos(\alpha_1)\cos(\alpha_3) + \cos(\alpha_2)\cos(\alpha_3)]. \end{aligned}$$

The commutation angles calculated for this technique are $\alpha_1 = 8.88^\circ$, $\alpha_2 = 27.59^\circ$, and $\alpha_3 = 50.54^\circ$. These were obtained using Matlab's Optimization Tool. Note that the optimal angle values are independent on the modulation index.

3.4 | Optimum nearest level

The conventional nearest level modulation (NLM) method has become popular among researchers due to its suitability for MLI applications^{13,16,27}. Compared with other low frequency modulation techniques, NLM does not need a complex calculation of the commutation angles (α_i), making the NLM method the simplest and most practical modulation method. In²⁷ Mohamed Ali et al. set the optimum nearest DC offset value to $0.4 V_{dc}$ in order to produce low THD and high rms voltage. The output voltage of the NLM method in terms of the number of levels and selection of the switching angle is expressed as:

$$V_{out} = m_i \left(\frac{L_{ph} - 1}{2} \right) V_{dc} \cdot \cos(\omega t), \quad (11)$$

where m_i is the modulation index and L_{ph} the number of level per phase. It is important to notice that the DC offset V_{dc} value variation is directly related to the switching angles (α_i). Calculation for the proposed ONLM is given in the following equation, the error is limited to $0.4 V_{dc}$ ²⁷:

$$\alpha_i = \arcsin \left(\frac{2(i - 0.6)}{L_{ph} - 1} \right), \text{ for } i = 1, 2, \dots, \left(\frac{L_{ph} - 1}{2} \right). \quad (12)$$

The commutation angles required to employ this technique are $\alpha_1 = 9.93^\circ$, $\alpha_2 = 10.64^\circ$, and $\alpha_3 = 66.88^\circ$.

4 | SIMULATION RESULTS

To properly compare the performance of the four presented modulation techniques, simulations with the same parameters are run using the Matlab/Simulink software. The evaluation criterion is based on the harmonic spectrum. The four modulation techniques can be divided into two implementation schemes: (i) square-shaped waveform, employed in the SHE, voltage (vTHD_{min}) and ONLM techniques and (ii) PWM waveform, utilized in the GSHE modulation. The proposed implementation schemes can be appreciated in Figures 4.(b) and 4.(c), respectively. Table 1 shows the circuit parameters used for the simulation. Three DC power sources are employed, producing an peak output voltage of 180 V. For the SHE and voltage vTHD_{min} technique, each cell commutates only twice during the entire period. In contrast, for gSHE approach commutates more that twice.

Table 1 Main circuit parameters for simulation.

Item	Symbol	Value
Cell Input Voltage	$V_{(A,i)}$	60 V
Phase Load	R	330 Ω
Power Frequency	f	60 Hz
Modulation Index	m_i	1 (–)

4.1 | SHE simulation analysis

Figure 9 shows the results obtained via simulation, employing the α_i angles obtained utilizing (7) and previously presented in Figure 6a. Figure 9b shows the harmonic spectrum of the line-to-line output voltage. It is vital to highlight the elimination of the 5th and 7th harmonics. Also, it is possible to see that the phase voltage THD is equal to 11.92%, and the line-to-line voltage THD is 7.61%. Therefore, the highest-value harmonic component in the line-to-line voltage harmonic spectrum is the 17th (4.6% of the fundamental part).

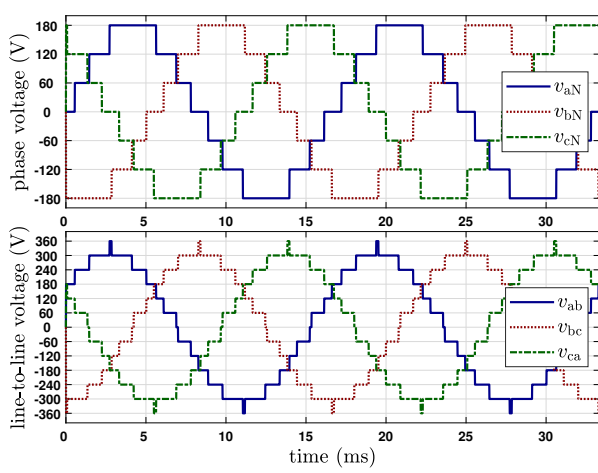
4.2 | gSHE simulation analysis

Figure 10 presents the simulation results obtained through the generalized SHE modulation technique. In Figure 10a, the phase voltage and line-to-line voltage waveforms can be observed. Besides, in Figure 10b the elimination of the 5th, 7th, 11th, 13th, 17th, 19th, 23rd, and 25th harmonics in the line-to-line voltage harmonic spectrum can be seen. The phase voltage THD is equal to 11.61%, and line-to-line voltage THD is 6.94%. The harmonic component with a higher magnitude is the 29th (4.8% of the fundamental component).

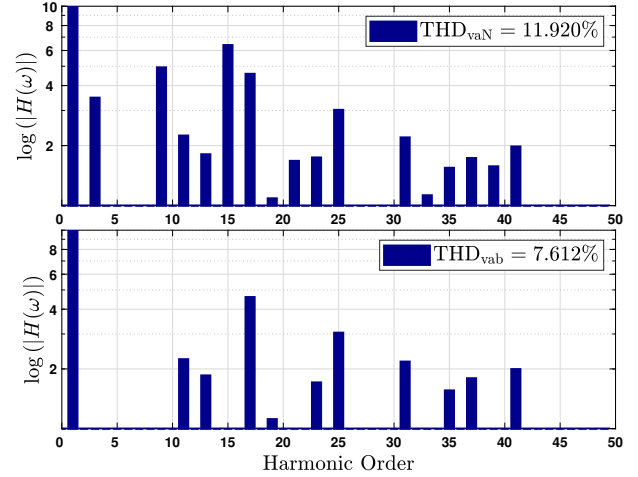
It is worth noticing that in this case, each level contains a notch, increasing the number of commutations per cycle. However, an improvement in the output voltage THD is achieved.

4.3 | Voltage THD Minimization (vTHD_{min}) simulation analysis

Similarly, the performance of the vTHD_{min} modulation technique is illustrated in Figure 11. Figure 11a shows the phase and line-to-line voltage waveforms. In both cases, the staircase waveform is obtained without notches. Figure 11b presents the harmonic

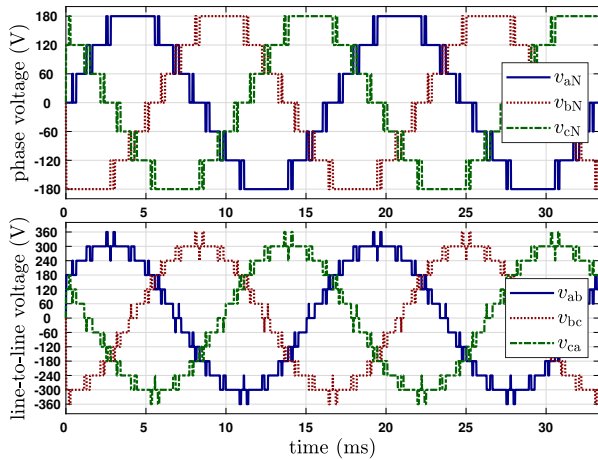


(a) Waveforms of the: (top) phase output voltage (v_{aN}, v_{bN}, v_{cN}), and (bottom) line-to-line output voltage (v_{ab}, v_{bc}, v_{ca}).

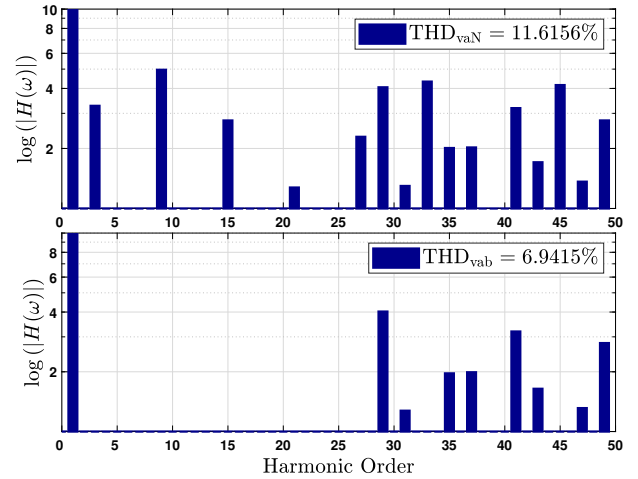


(b) Harmonic spectrum of the output voltage: (top) phase A voltage and (bottom) line-to-line voltage. Both are displayed in a logarithmic scale from 1% to 10%.

Figure 9 Simulation results of the SHE modulation technique, employing the parameters given in Table 1.



(a) Waveforms of the: (top) phase output voltage (v_{aN}, v_{bN}, v_{cN}), and (bottom) line-to-line output voltage (v_{ab}, v_{bc}, v_{ca}).



(b) Harmonic spectrum of the output voltage: (top) phase A voltage and (bottom) line-to-line voltage. The 5th, 7th, 11th, 13th, 17th, 19th, 23rd, and 25th harmonics in the line-to-line voltage are eliminated.

Figure 10 Simulation results of the gSHE modulation technique, employing the parameters given in Table 1

spectrum corresponding to the $v\text{THD}_{\min}$ modulation technique. The phase voltage THD is equal to 10.45% and the line-to-line voltage THD is equal to 9.69%. This technique does not wholly eliminate specific harmonics and reduces the harmonic magnitude to reach a minimum phase voltage THD. This strategy only guarantees the minimization of the phase voltage THD, but does not minimize the line-to-line voltage THD. This can be noticed in Figure 11b.

4.4 | ONLM simulation analysis

Finally, Figure 12a shows the phase and line-to-line voltage waveforms. Figure 12b shows the simulation results of the ONLM technique. The phase voltage THD is equal to 10.64% and the line-to-line voltage THD is 9.93%. This technique's objective is not to eliminate specific harmonics but achieves the elimination of the 5th and 11th harmonics unintentionally.

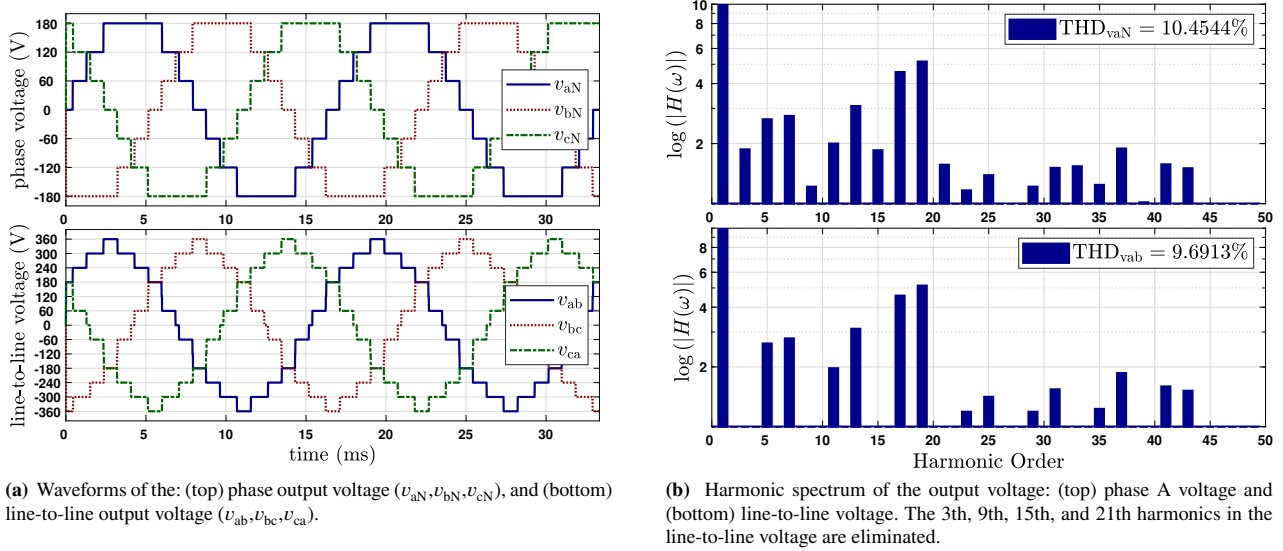


Figure 11 Simulation results of the SHE modulation technique, employing the parameters given in Table 1

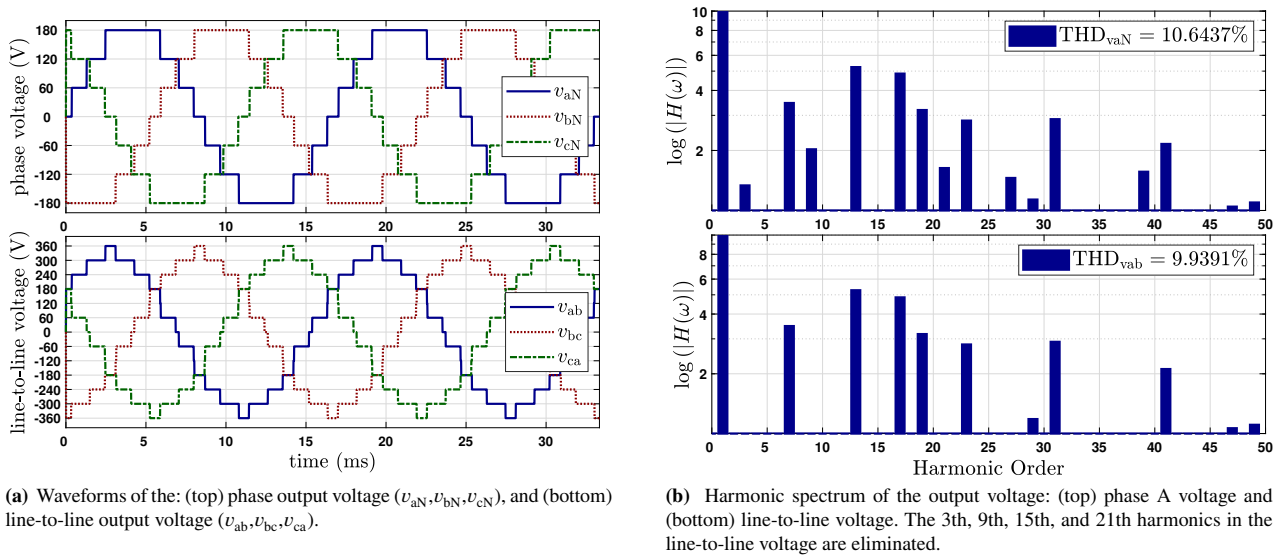


Figure 12 Simulation results of the SHE modulation technique, employing the parameters given in Table 1

5 | EXPERIMENTAL VALIDATION OF THE ANALYZED MODULATION TECHNIQUES

To validate the modulation mentioned above strategies, a lab-scale prototype was built. Figure 13 shows the prototype setup and Figure 14 details the power module's auxiliary circuits. The four modulation techniques have been tested and compared under the same circumstances and employed the parameters shown previously in Table 1. The waveforms and harmonic spectrum of the output voltage were captured employing a Fluke 437-II power quality and energy analyzer. Finally, the commanding signals have been generated using an FPGA from the family Artix7 to generate 36 PWM signals to control power modules. The effectiveness of the FPGA has been proved in similar applications²⁸.

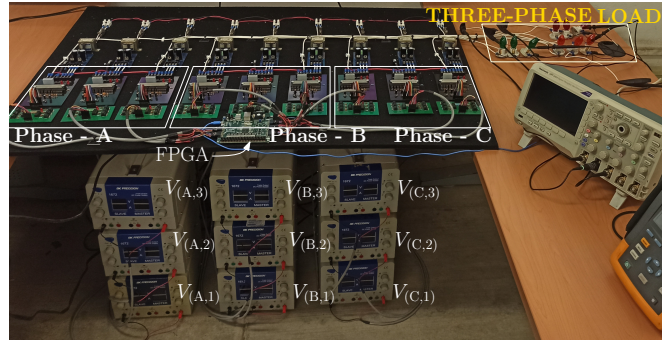


Figure 13 Photograph of the entire prototype of the CHB-MLI: each phase is composed of three power modules (HB), each with its corresponding DC power source ($V_{A,1-3}$, $V_{B,1-3}$, $V_{C,1-3}$). The setup of the prototype includes a three-phase load resistor.

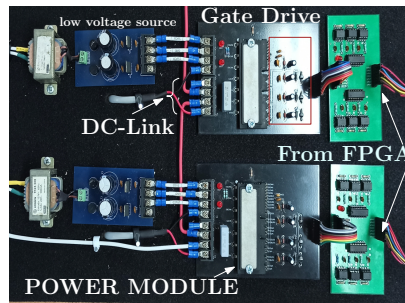


Figure 14 Photograph of two power modules with their gate drives included and interface from the FPGA Artix7.

5.1 | SHE experimental results

Figure 15 shows the experimental results obtained with the SHE modulation technique, which produces the commutation angles $\alpha_1 = 11.68^\circ$, $\alpha_2 = 31.17^\circ$ and $\alpha_3 = 58.57^\circ$. There is an excellent correspondence between the waveforms obtained by simulation in Figure 9 and the experimental waveforms of Figure 15. The simulation results show that the phase output voltage is a pure staircase waveform conformed by seven levels. Even though the line-to-line voltage contains narrowed steps, it reaches thirteen levels.

5.2 | gSHE experimental results

Figure 16 contains the waveforms and the harmonic spectra of the phase and line-to-line output voltage obtained when the generalized SHE modulation technique is employed. Unlike the conventional SHE technique, the gSHE technique utilizes more commutation angles that, in turn, generate notches at each level. The instantaneous waveforms can be appreciated in Figures 16a and 16c for the phase and line-to-line output voltage, respectively, whereas the spectrums are next to them. The THD in both cases is less than those obtained with the SHE technique. Nonetheless, the commutations are increased. The commutation angles are: $\alpha_1 = 8.04^\circ$, $\alpha_2 = 9.45^\circ$, $\alpha_3 = 13.61^\circ$, $\alpha_4 = 27.61^\circ$, $\alpha_5 = 32.25^\circ$, $\alpha_6 = 35.50^\circ$, $\alpha_7 = 54.08^\circ$, $\alpha_8 = 56.20^\circ$, and $\alpha_9 = 60.27^\circ$.

5.3 | $v\text{THD}_{\min}$ experimental results

The experimental results for the $v\text{THD}_{\min}$ technique can be visualized in Figure 17, which corroborates the theoretical simulation results. Compared to the SHE technique, the waveform shown in Figure 17a is a pure staircase without notches. However the harmonic spectrum and the THD value perform better.

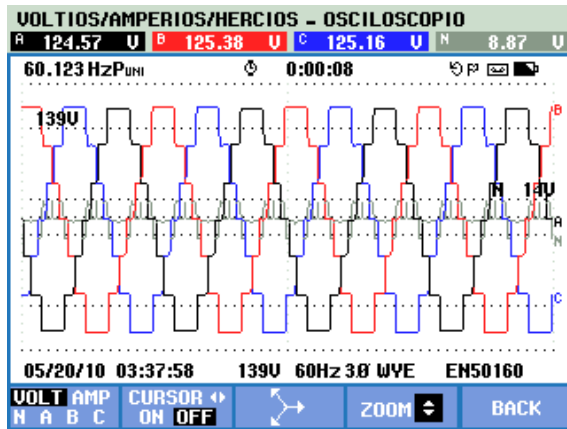
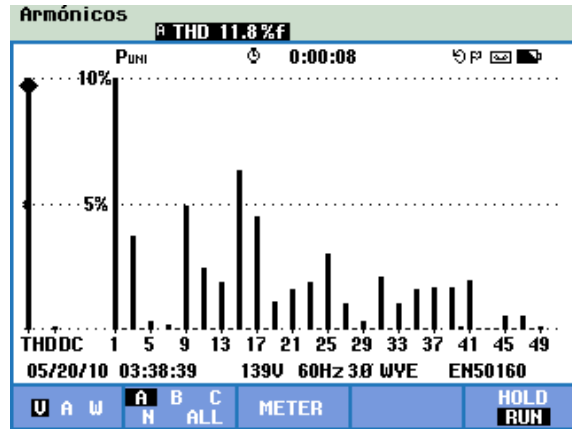
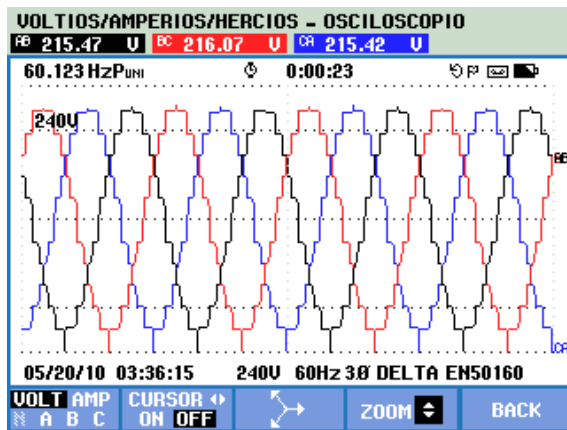
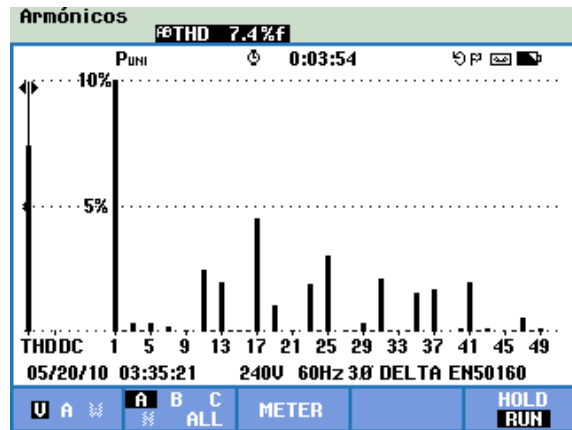
(a) Phase voltage waveforms (v_{aN}, v_{bN}, v_{cN}) with three optimal angles.(b) Harmonic spectrum at output phase voltage v_{aN} with THD = 11.8 %(c) Line-to-line voltage waveforms v_{ab}, v_{bc}, v_{ca} with three optimal angles.(d) Harmonic spectrum at output line-to-line voltage v_{ab} with THD = 7.4 %

Figure 15 Experimental results obtained with the SHE modulation technique for values of angles $\alpha_1 = 11.68^\circ$, $\alpha_2 = 31.17^\circ$ and $\alpha_3 = 58.57^\circ$. The waveform is a staircase type.

5.4 | ONLM experimental results

Finally, Figure 18 presents the experimental results of the Optimum Nearest Level Modulation technique. In all cases, theoretical and experimental results agree. Similar to the SHE, and $vTHD_{min}$ techniques the ONL modulation employs three angles per quarter of cycle, keeping the commutations low however, the THD is not the lowest.

6 | MODULATION TECHNIQUES COMPARISON

In this section, the results obtained with the modulation above methods are compared under the same conditions. Table 2 summarizes the number of angles with their corresponding number of commutations per fundamental period. Also, a comparison between the ideal and the actual THD for the four techniques is included. The phase voltage and the line-to-line voltage have been measured from v_{aN} and v_{ab} , respectively, along with the THD values.

In Table 2 it is important to notice that the GSHE technique has the lowest THD values, this is why this technique has been chosen as the best option for this work.

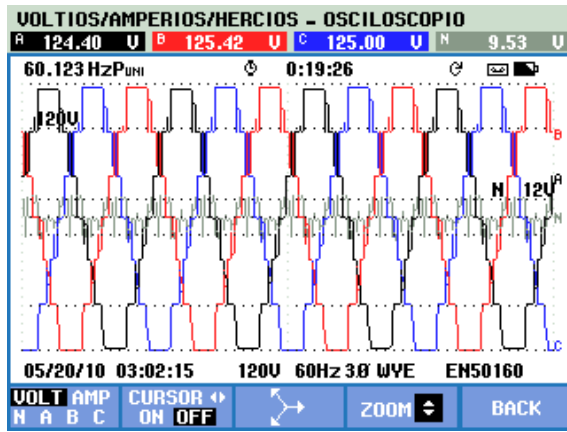
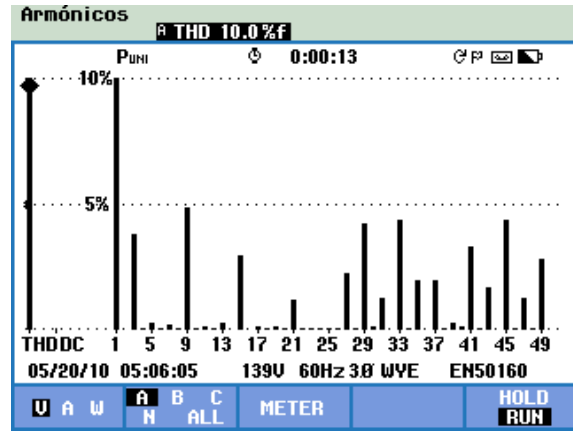
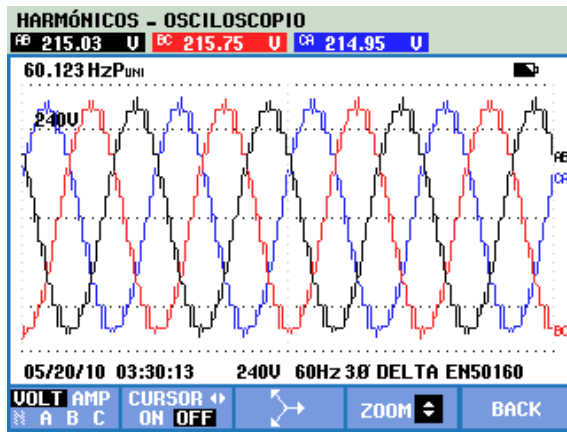
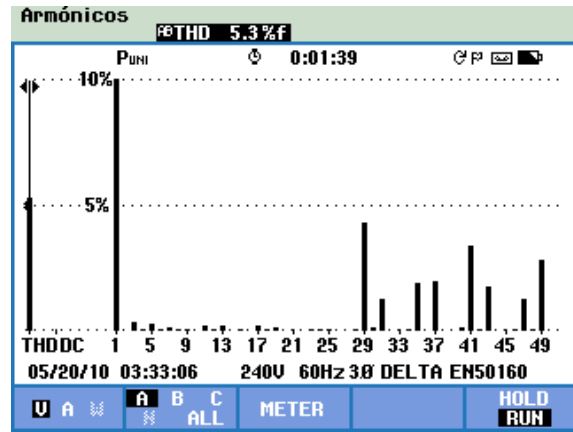
(a) Phase voltage waveforms (v_{aN}, v_{bN}, v_{cN}) with nine optimal angles.(b) Harmonic spectrum at output phase voltage (v_{aN}) with THD =10.0 %(c) Line-to-line voltage waveforms v_{ab}, v_{bc}, v_{ca} with 3 optimal angles.(d) Harmonic spectrum at output line-to-line voltage (v_{ab}), THD =5.3 %

Figure 16 Experimental results obtained with the generalized SHE modulation technique with nine angle values. The waveform is a staircase with notches.

Table 2 Modulation techniques comparison.

Parameter	Modulation Techniques			
	SHE	GSHE	vTHDmin	ONLM
Number of Commutations	12	36	12	12
Number of angles α_i	3	9	3	3
THD _{vab} (simulated)	7.61	6.94	9.69	9.93
THD _{vab} (experimental)	7.40	5.30	9.50	9.60
THD _{vaN} (simulated)	11.92	11.61	10.45	10.64
THD _{vaN} (experimental)	11.80	10.00	10.20	10.30

7 | CONCLUSIONS

The four different modulation techniques were analyzed and applied to compute the commutation angles. Then, their effectiveness was corroborated numerically and experimentally. As it was demonstrated in this article, there are currently several low-frequency commutation modulation techniques, each with its features. Choosing the one that is more adequate will depend

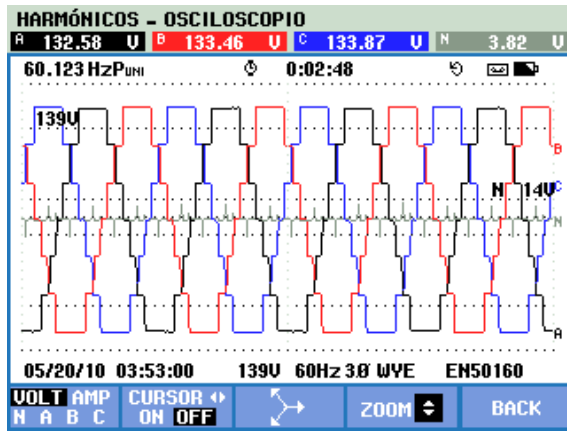
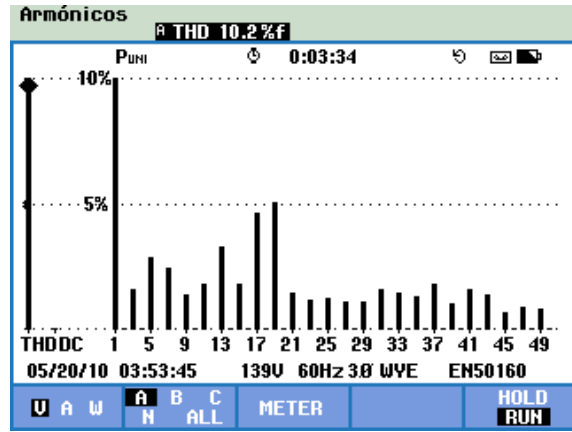
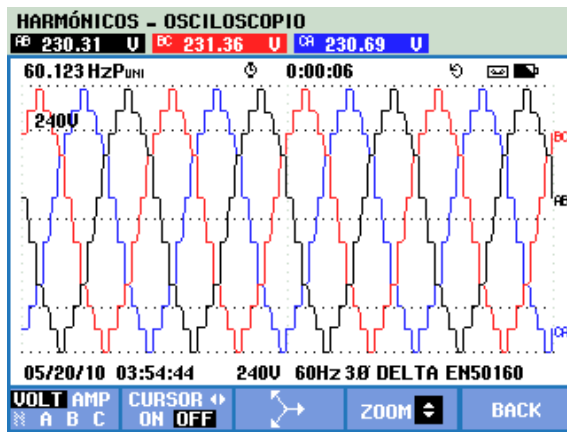
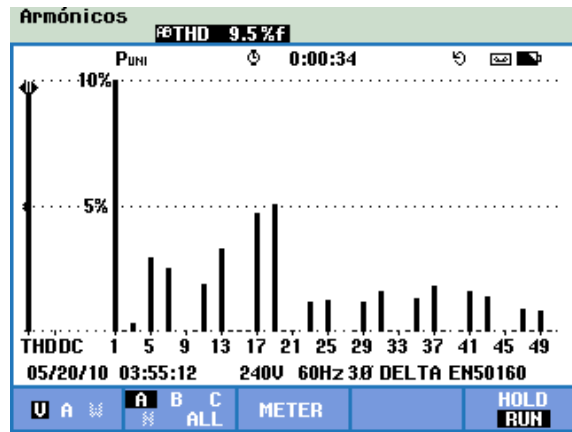
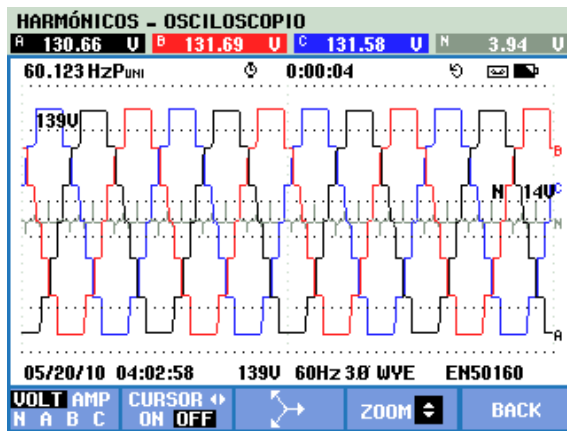
(a) Phase voltage waveforms (v_{aN}, v_{bN}, v_{cN}) with nine optimal angles.(b) Harmonic spectrum at output phase voltage (v_{aN}), THD = 10.2 %(c) Line-to-line voltage waveforms (v_{ab}, v_{bc}, v_{ca}) with three optimal angles.(d) Harmonic spectrum at output line-to-line voltage (v_{ab}) with THD = 9.5 %

Figure 17 Experimental results obtained with the voltage THD minimization ($vTHD_{min}$) modulation technique with three angle values: $\alpha_1 = 8.882^\circ$, $\alpha_2 = 27.596^\circ$, and $\alpha_3 = 50.541^\circ$. The waveform is a staircase with notches.

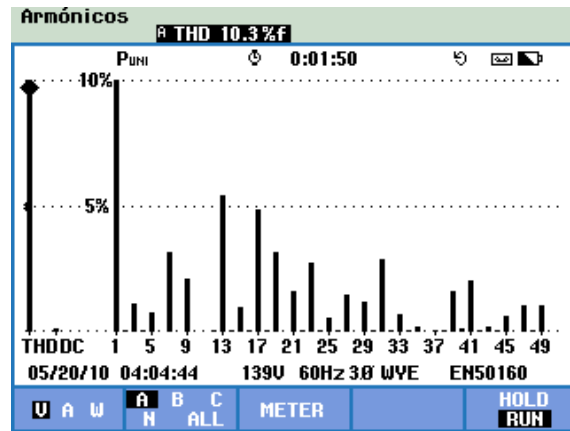
on the application in which the multilevel inverter is located. Considering the results obtained in the harmonic spectra corresponding with the line-to-line voltage (for the SHE, gSHE, and minTHD techniques, which contain a THD of 7.61%, 6.94, and 9.69%, respectively) it is suggested the use of the generalized SHE as the best choice. It is worth mentioning that, while the generalized SHE is the best alternative, locating the commutation angles becomes a complicated task for a microcontroller or digital signal processor (DSP), this is the reason why it is suggested the use of an FPGA and the implementation of an optimization algorithm to assure that the commutation angles are optimal.

References

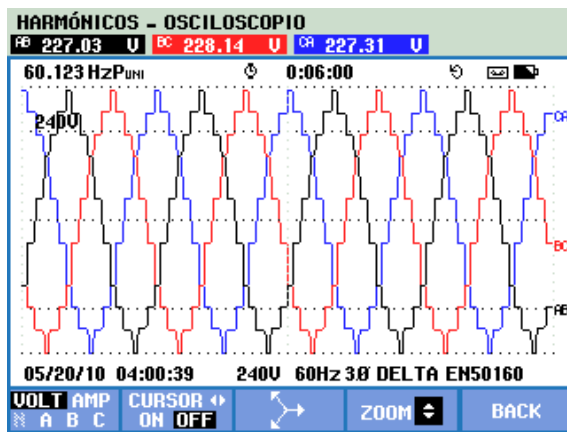
1. Rodriguez J, Franquelo L, Kouro S, et al. Multilevel Converters: An Enabling Technology for High-Power Applications. *Proceedings of the IEEE* 2009; 97(11): 1786–1817. doi: 10.1109/JPROC.2009.2030235
2. Vasu R, Chattopadhyay SK, Chakraborty C. Asymmetric Cascaded H-Bridge Multilevel Inverter With Single DC Source per Phase. *IEEE Transactions on Industrial Electronics* 2020; 67(7): 5398–5409. doi: 10.1109/TIE.2019.2934080
3. Sedaghati F, Majareh SHL. A multilevel inverter based on cascade connection of submultilevel units with reduced switch count. *International Journal of Circuit Theory and Applications* 2019; 47(7): 1152–1172. doi: <https://doi.org/10.1002/cta.2638>



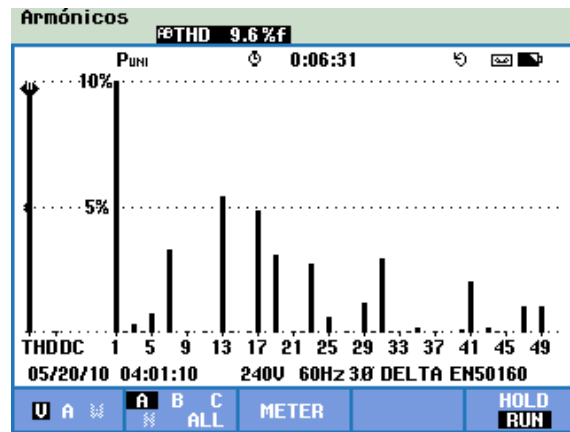
(a) Phase voltage waveforms (v_{aN}, v_{bN}, v_{cN}) with nine optimal angles.



(b) Harmonic spectrum at output phase voltage (v_{aN}) with THD = 10.2 %



(c) Line-to-line voltage waveforms (v_{ab}, v_{bc}, v_{ca}) with three optimal angles.



(d) Harmonic spectrum at output line-to-line voltage (v_{ab}) with THD = 9.5 %

Figure 18 Experimental results obtained with the voltage Optimum Nearest Level Modulation (ONL) modulation technique with three angle values: $\alpha_1 = 7.66^\circ$, $\alpha_2 = 27.81^\circ$, and $\alpha_3 = 53.13^\circ$. The waveform is pure staircase.

4. Pourjafar S, Shayeghi H, Sedaghati F, Seyedshenava S, Blaabjerg F. A bidirectional multiport DC-DC converter applied for energy storage system with hybrid energy sources. *International Journal of Circuit Theory and Applications* 2021; 49(8): 2453-2478. doi: <https://doi.org/10.1002/cta.2988>
5. Bana PR, Panda KP, Naayagi RT, Siano P, Panda G. Recently Developed Reduced Switch Multilevel Inverter for Renewable Energy Integration and Drives Application: Topologies, Comprehensive Analysis and Comparative Evaluation. *IEEE Access* 2019; 7: 54888-54909. doi: 10.1109/ACCESS.2019.2913447
6. S. S, Sathyan S. A three-level three port isolated converter with reduced current stress for DC microgrid applications. *International Journal of Circuit Theory and Applications*; n/a(n/a). doi: <https://doi.org/10.1002/cta.3572>
7. Kouro S, Malinowski M, Gopakumar K, et al. Recent Advances and Industrial Applications of Multilevel Converters. *IEEE Transactions on Industrial Electronics* 2010; 57(8): 2553-2580. doi: 10.1109/TIE.2010.2049719
8. Alishah RS, Hosseini SH, Babaei E, Sabahi M. A new single-phase multilevel converter topology with reduced power electronic devices, voltage rating on switches, and power losses. *International Journal of Circuit Theory and Applications* 2018; 46(7): 1372-1391. doi: 10.1002/cta.2484

9. Abu-Rub H, Holtz J, Rodriguez J, Ge Baoming . Medium-Voltage Multilevel Converters—State of the Art, Challenges, and Requirements in Industrial Applications. *IEEE Transactions on Industrial Electronics* 2010; 57(8): 2581–2596. doi: 10.1109/TIE.2010.2043039
10. Omer P, Kumar J, Surjan BS. A Review on Reduced Switch Count Multilevel Inverter Topologies. *IEEE Access* 2020; 8: 22281–22302. doi: 10.1109/ACCESS.2020.2969551
11. Turnbull FG. Selected harmonic reduction in static D-C — A-C inverters. *IEEE Transactions on Communication and Electronics* 1964; 83(73): 374-378. doi: 10.1109/TCOME.1964.6541241
12. Vijeh M, Rezanejad M, Samadaei E, Bertilsson K. A General Review of Multilevel Inverters Based on Main Submodules: Structural Point of View. *IEEE Transactions on Power Electronics* 2019; 34(10): 9479–9502. doi: 10.1109/TPEL.2018.2890649
13. Siddique MD, Iqbal A, Sarwar A, Mekhilef S. Analysis and implementation of a new asymmetric double H-bridge multilevel inverter. *International Journal of Circuit Theory and Applications* 2021; 49(12): 4012-4026. doi: <https://doi.org/10.1002/cta.3091>
14. Nageswar Rao B, Suresh Y, Shiva Naik B, Venkataramanaiah J, Aditya K, Kumar Panda A. A novel single source multilevel inverter with hybrid switching technique. *International Journal of Circuit Theory and Applications* 2022; 50(3): 794-811. doi: <https://doi.org/10.1002/cta.3196>
15. Samadaei E, Sheikholeslami A, Gholamian SA, Adabi J. A Square T-Type (ST-Type) Module for Asymmetrical Multilevel Inverters. *IEEE Transactions on Power Electronics* 2018; 33(2): 987-996. doi: 10.1109/TPEL.2017.2675381
16. Arif MSB, Sarwer Z, Siddique MD, Md. Ayob S, Iqbal A, Mekhilef S. Asymmetrical multilevel inverter topology with low total standing voltage and reduced switches count. *International Journal of Circuit Theory and Applications* 2021; 49(6): 1757-1775. doi: <https://doi.org/10.1002/cta.2971>
17. Erickson RW, Maksimovic D. *Fundamentals of Power Electronics*. Kluwer Academic Publishers . 2001.
18. Fei W, Ruan X, Wu B. A Generalized Formulation of Quarter-Wave Symmetry SHE-PWM Problems for Multilevel Inverters. *IEEE Transactions on Power Electronics* 2009; 24(7): 1758–1766. doi: 10.1109/TPEL.2009.2018094
19. Khamooshi R, Namadmalan A. Converter utilisation ratio assessment for total harmonic distortion optimisation in cascaded H-bridge multi-level inverters. *IET Power Electronics* 2016; 9(10): 2103–2110. doi: 10.1049/iet-pel.2015.0787
20. Najjar M, Moeini A, Bakhshizadeh MK, Blaabjerg F, Farhangi S. Optimal Selective Harmonic Mitigation Technique on Variable DC Link Cascaded H-Bridge Converter to Meet Power Quality Standards. *IEEE Journal of Emerging and Selected Topics in Power Electronics* 2016; 4(3): 1107–1116. doi: 10.1109/JESTPE.2016.2555995
21. Konstantinou G, Agelidis VG, Pou J. Theoretical Considerations for Single-Phase Interleaved Converters Operated With SHE-PWM. *IEEE Transactions on Power Electronics* 2014; 29(10): 5124–5128. doi: 10.1109/TPEL.2014.2319826
22. Iqbal A, Meraj M, Tariq M, Lodi KA, Maswood AI, Rahman S. Experimental Investigation and Comparative Evaluation of Standard Level Shifted Multi-Carrier Modulation Schemes With a Constraint GA Based SHE Techniques for a Seven-Level PUC Inverter. *IEEE Access* 2019; 7: 100605–100617. doi: 10.1109/ACCESS.2019.2928693
23. Saeedian M, Adabi J, Hosseini SM. Cascaded multilevel inverter based on symmetric–asymmetric DC sources with reduced number of components. *IET Power Electronics* 2017; 10(12): 1468-1478. doi: <https://doi.org/10.1049/iet-pel.2017.0039>
24. Niknam Kumle A, Fathi SH, Jabbarvaziri F, Jamshidi M, Heidari Yazdi SS. Application of memetic algorithm for selective harmonic elimination in multi-level inverters. *IET Power Electronics* 2015; 8(9): 1733–1739. doi: 10.1049/iet-pel.2014.0209
25. Agelidis VG, Balouktsis AI, Dahidah MSA. A Five-Level Symmetrically Defined Selective Harmonic Elimination PWM Strategy: Analysis and Experimental Validation. *IEEE Transactions on Power Electronics* 2008; 23(1): 19–26. doi: 10.1109/TPEL.2007.911770

26. Yousefpoor N, Fathi SH, Farokhnia N, Abyaneh HA. THD Minimization Applied Directly on the Line-to-Line Voltage of Multilevel Inverters. *IEEE Transactions on Industrial Electronics* 2012; 59(1): 373–380. doi: 10.1109/TIE.2011.2143373
27. Mohamed Ali JS, Alishah RS, Krishnasamy V. A New Generalized Multilevel Converter Topology With Reduced Voltage on Switches, Power losses, and Components. *IEEE Journal of Emerging and Selected Topics in Power Electronics* 2019; 7(2): 1094–1106. doi: 10.1109/JESTPE.2018.2886214
28. Rahul JR, Annamalai K. FPGA-based implementation of single-phase seven-level quasi-Z-source inverter. *International Journal of Circuit Theory and Applications* 2019; 47(12): 1970-1989. doi: <https://doi.org/10.1002/cta.2709>

AUTHOR BIOGRAPHY

empty-eps-converted-to-pdf	<p>Juan H. Almazan Covarrubias. Almazan Covarrubias is currently pursuit its PhD in the Instituto Tecnológico de Cd. Madero, he received the B.S. degree in electronics engineering from Instituto Tecnológico de Cd. Madero. He has over 16 years of Managerial Experience in the academic setting His research interests include modeling and control of power electronics converters and their application to utility scale power systems.</p>
empty-eps-converted-to-pdf	<p>Pedro Martín García-Vite. Pedro Martín Garcia-Vite received the B.S. degree in electronics and the M.S. degree in electrical engineering from Instituto Tecnológico de Cd. Madero in 2004 and 2006, respectively, and his Ph.D. degree in electrical engineering from the Centro de Investigación y de Estudios Avanzados del Instituto Politécnico Nacional, Guadalajara, México, in 2012. He is currently with the Tecnológico Nacional de México-Instituto Tecnológico de Cd. Madero. His research interests include modeling and control of power electronics converters and their application to utility scale power systems.</p>
empty-eps-converted-to-pdf	<p>Juan M. Ramirez. Professor Juan M. Ramirez received a Ph.D. in electrical engineering from Universidad Autonoma de Nuevo Leon, Mexico, in 1992. He joined the Department of Electrical Engineering, CINVESTAV, Guadalajara, Mexico, in 1999 and is currently a full-time Professor. His research interests include smart grids, microgrids, and power electronics applications.</p>
<p>How to cite this article: Almazán Covarrubias, J. H., García Vite, P. M., and Ramírez Arredondo, J. M. (2023), Comparison of Low-Frequency-Commutation Modulation Techniques in a Symmetrical Cascaded H-Bridge Multilevel Inverter, <i>Q.J.R. Meteorol. Soc.</i>, 2023;00:1–6.</p>	