A Capacitive Mismatch Calibration Method for SAR ADCs Based on TDC

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The capacitance mismatch problem limits the accuracy improvement of high-precision SAR ADCs (Successive Approximation Register Analog-to-Digital Converters). To address the capacitance array mismatch in SAR ADCs, this paper proposes a novel capacitor calibration scheme based on the Time-to-Digital Converter (TDC). This scheme achieves calibration accuracy as high as 0.01% and can be flexibly designed to meet the accuracy requirements of SAR ADCs. Simulation results indicate that the capacitance mismatch issue of a redundant capacitor 13-bit SAR ADC can be completely eliminated, and the effective number of bits (ENOB) can approach the ideal value of 13.18 bits. Additionally, the analog component of this scheme utilizes four inverter chains, two D flip-flops, and four counters, without requiring a large area for auxiliary calibration capacitors.

Introduction: It is well known that SAR ADCs have nonlinearities due to capacitance mismatch, which makes it difficult to improve the accuracy. In order to improve the SNDR (Signal-to-Noise and Distortion Ratio) of SAR ADCs, many design methods for capacitor calibration have been proposed in the industry. The method of using auxiliary calibration capacitors [1, 2] can gradually calibrate the higher capacitance, but the area of the capacitor array increases after adding the auxiliary capacitors, and the parasitics also increase, in addition to its accuracy is limited by the smallest bit capacitance. LMS (Least Mean Squares) algorithm to calibrate the capacitance mismatch is currently the mainstream method to improve the accuracy [3–7], such as high-precision low-speed ADC to calibrate the high-speed SAR ADC, the two SAR ADCs to calibrate each other, PN (pseudorandom) injected signals to extract the mismatch signal and other methods. The LMS algorithm to calibrate the capacitance mismatch requires a large number of iterative calculations, which need to store a large amount of historical data resources, and the number of its convergence is tens of thousands of times, so it occupies a large number of storage resources and is more troublesome to apply. There is another method used to reduce the effect of capacitance mismatch, DEM [8](Dynamic Element Matching), by controlling each unit capacitance, to disrupt the fixed capacitance mismatch, if you use conventional capacitor arrays, the control switches need to be 2^N, N is the number of bits of capacitance arrays, so it is necessary to use the R-C DAC(Resistor-Capacitor Digital-to-Analog Converter) arrays in order to reduce the number of units of capacitance, for high-precision ADCs there will be a very large number of control switches. Using the histogram calibration method [9] requires a high-quality triangular wave to be generated first, which requires large capacitors and op-amps, which contradicts the purpose of low power consumption of SAR ADCs, and at the same time, it requires a lot of computation and a number of convergences. The method of using an RC filter curve to measure a histogram[10] can eliminate the need for large capacitors and operational amplifiers. However, its processing involves a significant amount of logarithmic and square root calculations, resulting in a high computational workload. Whereas in this project only minimal hardware as well as computation is used to measure the capacitance mismatch and also flexibility to design its accuracy according to the application.

The proposed TDC-based measurement mismatch scheme: The schematic diagram of the calibration mode is shown in Figure 1. The sampling switch is turned off, and the CDAC(Capacitive Digital-to-Analog Converter) array is controlled only by SAR logic. The SAR ADC architecture used in this project is a KT/C noise-eliminating structure [11]. The difference voltage at the input end of the comparator is measured by the time domain comparator and converted into a pair of signals with phase difference, and then the specific phase difference is measured by TDC, and the difference voltage can be back-derived. According to this principle, the capacitor array is first controlled to produce a 1LSB voltage difference, and then the result measured by TDC is used as a reference. Based on this reference, the voltage with each bit mismatch information can be generated and measured by controlling capacitor array switching. Finally, the mismatch information of each capacitor is obtained. The calibration mode is then terminated and the conversion is performed as a normal SAR ADC when it enters normal operating mode.

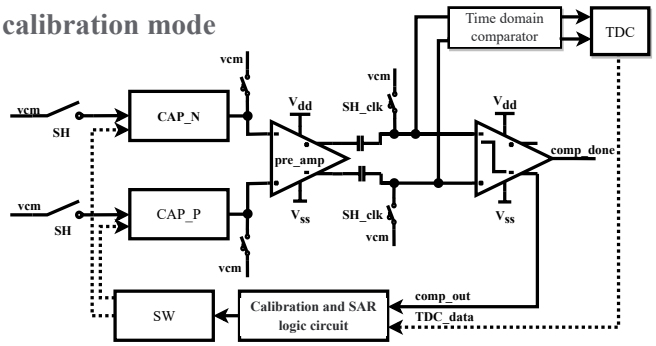
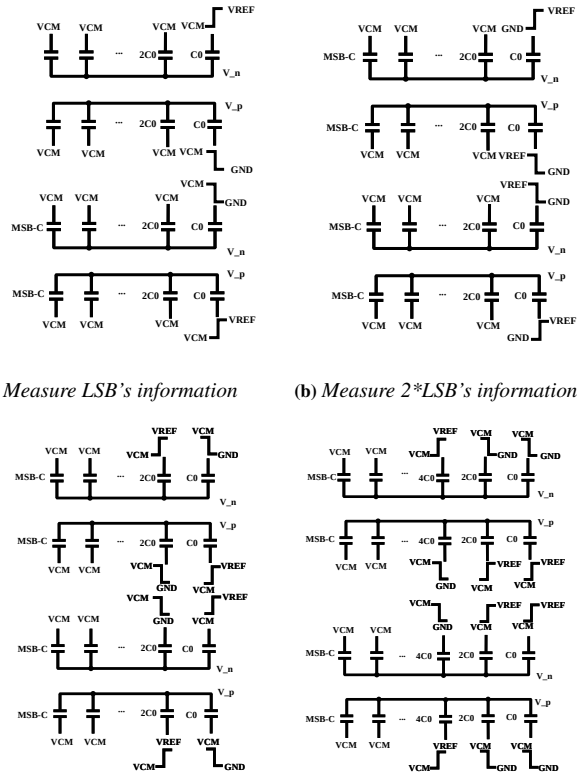


Fig 1 *Schematic diagram of the ADC in calibration mode.*



(a) *Measure LSB's information* **(b)** *Measure 2*LSB's information*

(c) *Measure the actual weight of 2*C0* **(d)** *Measure the actual weight of 4*C0*

Fig 2 *Detection process.*

Detection process: In order to remove the PVT effect of the TDC, the time domain comparator and TDC are first used to measure the LSB voltage corresponding information of the CDAC array. The control of the CDAC array is shown in Figure 2. Figure 2(a) shows that both the upper and lower plates of the CDAC array are reset to VCM during reset. After the reset, the lower plate of the LSB capacitor changes from VCM to GND or VREF. Due to the mismatch between the time domain comparator and the TDC, the positive and negative LSB voltages need to be measured twice respectively, and the information of these two voltages can be used to obtain the result without mismatch.

Then the information of twice LSB voltage is measured as in Figure 2(b). In the reset stage, the CDAC upper boards are all reset to VCM, the CDAC lower boards except the LSB capacitor are also reset to VCM,

and the LSB capacitor lower boards are reset to GND, VREF. After the reset is completed, the CDAC upper boards disconnect the reset switch, and the LSB lower boards are changed from GND to VREF and VREF to GND. At this time, the CDAC upper boards' voltages are changed to twice the LSB voltage. Similarly, in order to eliminate the effect of offset, two times the LSB voltage is detected. Once you get the LSB voltage as well as the 2LSB voltage, you can get information about the TDC output corresponding to the voltage on the CDAC upper board.

For example, in Figure 2 (c), when measuring the specific capacity of the 2*C0 capacitor. During the reset, both the CDAC upper board and lower board are reset to VCM. After the reset, the lower board of the measured capacitor changes from VCM to GND, VREF, and the LSB capacitor changes from VCM to VREF, GND. At this point, if there is no capacitor mismatch, the voltage difference of the parent board should be an LSB voltage. However, due to process deviation, the voltage on the upper board may not be 1LSB, but there will be a slight deviation. The information of this voltage difference can be measured by TDC, to obtain the specific information of the mismatch, and push back the specific weight value of the 2C0 capacitor. The actual weight for measuring the higher capacitance is also the same as in the above process. As shown in Figure 2(d), when measuring 4C0, the control reset and the capacitor control switch after the reset are performed. Since 2C0 already knows the specific weight, it can directly use its actual weight value to calculate the actual weight of 4C0 at this time.

When testing capacitors, only the weight difference between the measured capacitor and the known capacitor weight is close to 1LSB voltage, then the weight deviation can be accurately measured. Errors may increase if it is much larger than 1LSB.

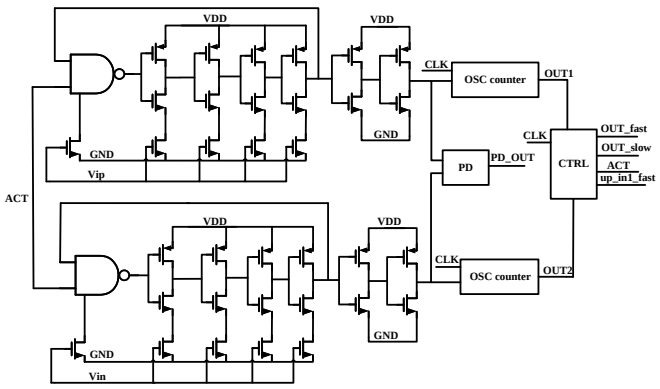


Fig 3 *Time domain comparator schematic.*

Time-domain comparator that outputs a phase difference signal: Figure 3 is a changed version of the oscillator-based time-domain comparator [12]. Input differential voltage Vip and Vin, due to the different voltage sizes, the control current on the current limiting NMOS tube is different, so the signal through the upper and lower voltage control delay chain delay is different, which will lead to a certain phase difference. After the Vin and Vin are established and the ACT signal is enabled, the upper and lower signals will be generated, and the phase difference will be enlarged after repeated oscillation. The number of oscillations can be calculated through the counter, and the fixed oscillation count is specified. When the oscillation count is reached, the upper and lower two delay chains output a rising edge signal respectively. The phase difference of the two rising edge signals is proportional to the input differential voltage, so the information on the input differential voltage can be obtained as long as the phase difference is measured by TDC. PD (phase discriminator) can output the positive and negative polarity of the Vin. CTRL processes the two rising edge signals output by the counter and determines which one is the leading signal OUT_fast and which is the lagging signal OUT_slow, which is convenient for the subsequent TDC to measure the phase difference. These two rising edge signals can be detected at the same time. For example, when detecting the rising edge of the OUT1 signal, if OUT2 is still low, it means that the OUT1 signal is the leading signal OUT_fast, and the rising edge signal OUT_fast is output at this time, and the output signal up_in1_fast represents that OUT1 signal is the leading signal. So that the TDC can be used to eliminate the imbalance. If OUT2 is high, OUT1 is the lagging signal OUT_slow, and the rising edge signal OUT_slow is output at this time. The same procedure is used to detect the rising edge of the OUT2 signal. At the same time, CTRL generates a signal for the start of the oscillation ACT. And stops the oscillation after the number of oscillations is reached to reduce the dynamic power consumption.

However, this structure determines that the process deviation will greatly affect the phase difference size of the output, and even may lead to the direct opposite of positive and negative polarity due to the process deviation. For example, Vip should have been greater than Vin, but due to mismatch, the delay of the upper voltage delay controller chain is larger, resulting in the rising edge of the output of the upper delay controller chain when it reaches a certain number of turns, but lagging behind the output below. To eliminate the influence of the imbalance, it is necessary for Vip and Vin to work once in the upper and lower two delay chains respectively, and the correct polarity and the phase difference size without imbalance can be obtained according to the results of the two-phase differences. The specific way to deal with phase differences is described in the TDC principle section.

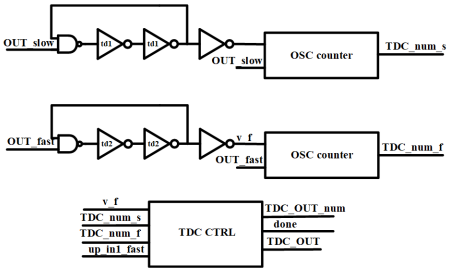


Fig 4 *Schematic diagram of TDC.*

The proposed oscillator-based TDC: The TDC shown in Figure 4 receives a pair of rising edge signals with a phase difference as its inputs from the time-domain comparator. The signal OUT_fast, which is phase-leading, passes through a longer delay chain (td2), while the signal OUT_slow, which is phase-lagging, passes through a shorter delay chain (td1). After some time, the OUT_slow signal catches up with the OUT_fast signal. The moment when the oscillation counts of the two delay loops are equal represents the capturing point, which contains the phase difference information. The TDC CTRL checks whether the counts are equal at each arrival of the oscillation signal. If they are equal, it outputs the result TDC_OUT_num, the polarity signal TDC_OUT, and generates a completion signal 'done' to control the termination of the oscillation. Similarly, the mismatch between the upper and lower delay chains of the TDC can also lead to incorrect results. Therefore, a calibration for offset should be performed together with the time-domain comparator.

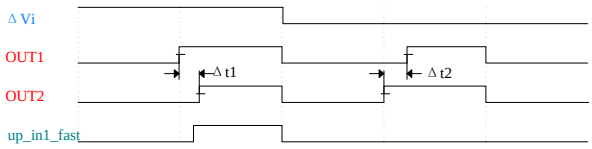
Mismatch Calibration Scheme: Due to process deviations, the actual delay times of the upper and lower delay chains are not always the same. As shown in Figure 2 by controlling the CDAC capacitor switch to measure the positive input differential voltage once, and then measure the negative differential voltage once, from these two results will be able to get the correct final result.

Control input Vip-Vin first positive and then negative, the upper and lower two inverter chain process deviation is not too large as shown in Figure 5 (a), OUT1 will initially lead OUT2 and then lag behind OUT2, meaning that up_in1_fast will first output a high level and then a low level. At this time, the output result of the first TDC is defined as TDC_num_first, and the output result of the second TDC is defined as TDC_num_second. At this time the results of the

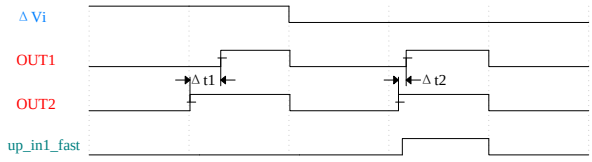
$$TDC\_num\_total = (TDC\_num\_first + TDC\_num\_second)/2.$$

When the upper inverter chain is too slow and the lower one is too fast, as shown in Figure 5(b), This will result in an incorrect second judgment, as both outputs of up_in1_fast will be >0. The first TDC output, TDC_num_first, is larger, while the second TDC output is the negation of the actual value. Therefore, the actual result is:

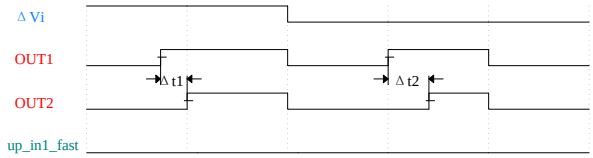
$$TDC\_num\_total = (TDC\_num\_first - TDC\_num\_second)/2.$$



(a) *The phase shift difference between the two delay chains is not large*



(b) *The upper delay chain is slower*



(c) *The top delay chain is faster*

Fig 5 *Timing diagram for calibration of critical voltages.*

Similarly, when the upper inverter chain is too fast and the lower one is too slow, as shown in Figure 5(c), it will result in an incorrect first judgment, where both up_in1_fast output low-level signals. The actual result is then:

$$TDC\_num\_total = (TDC\_num\_second - TDC\_num\_first)/2.$$

The same derivations apply when the input voltage Vip-Vin is negative first and then positive. Based on the LSB voltage and the measured LSB_num and LSB_2_num for 2*LSB voltage, the slope and intercept formulas for the general linear equation concerning the voltage on the CDAC upper board can be obtained as follows.

$$k = 1/(LSB\_num\_2 - LSB\_num).$$

$$b = (LSB\_num\_2 - 2 * LSB\_num)/(LSB\_num\_2 - LSB\_num).$$

$$V = k * TDC\_num\_total + b.$$

Based on these formulas, it is possible to reverse-calculate the input differential voltage, and subsequently deduce the specific weight values of the capacitors. Because only one set of formula parameters and the actual weights of the capacitors need to be stored, the computational workload is very small, and there is no need for a large storage circuit.

simulation result: To verify the feasibility, a Monte Carlo simulation was performed using a 13-bit SAR ADC. In order to shorten the simulation time, the sampling circuit and amplifier of the SAR ADC were modeled using Verilog-A, while the capacitors, time-domain comparators, and TDC were simulated using Monte Carlo models with actual capacitor and transistor models for the 65nm process. Before and after the calibration, the SNDR of the ADC was compared. Figure 6 shows the comparison of effective bit numbers before and after calibration, demonstrating the effectiveness of this calibration scheme. From the figure, it can be observed that under different mismatch conditions, the effective bit numbers after calibration are close to the ideal value of 13 bits. The SNDR and SFDR have improved significantly. Because the mismatch of the capacitor is determined after manufacturing and does not change with PVT, the weight value can be stored after one calibration. In this case, the average calibration time is 30 us. After that, the mismatch calibration of the capacitor is not required, so the power consumption and speed of the original SAR ADC will not be affected.

Conclusion: This paper proposes a new capacitor mismatch calibration method based on TDC, which does not require a large number of auxiliary capacitor arrays, nor a large number of storage resources and

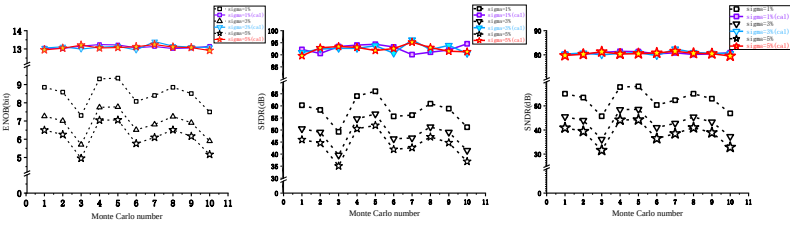


Fig 6 *Monte Carlo result.*

computing resources, but only needs to add some inverter, D flip-flop, counter, and other digital circuits, which is very conducive to the design and process iteration of low power domain, thereby reducing power consumption. Adjusting the time domain comparator flipping times can also flexibly adjust the calibration accuracy. Ideal for high-precision SAR ADC calibration or medium to low-precision applications with very high area and power requirements.

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